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H55H-LAIO

For MXM

Rev:1.0

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PAGE 41 HISTORY

The IbexPeak module Specification :

- 1. MEMORY : 4 channel SO-DIMM DDR3 socket
- 2. SLOT : 2 MINI PCI-E by 1
- 3. With 11 port Usb 2.0 & 2 port S-ATAII , 1 port eS-ATAII
- 4. LAN : INTEL LAN 82578DC 1000M
- 5. AUDIO : REALTEK ALC662/ALC888 Audio Codec
- 6. I/O : Super I/O ITE 8721 with PS2 KB
- 7. VIDEO : RTD2120 + RTD2555 & MXM 3.0 Card

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PCH GPIO Function

Signal Name	Type	Voltage	Default	Functional Description	Net name
GPIO1	I/O	3.3 V	GPI	Touch sensor Led Control	FRONT_LED
GPIO2	I/OD	3.3 V	GPI	Touch sensor Volume UP Control	VOL_UP
GPIO3	I/OD	3.3 V	GPI	Touch sensor Volume Down Control	VOL_DOWN
GPIO4	I/OD	3.3 V	GPI	Touch sensor Bright up Control	BRIGHT_UP
GPIO5	I/OD	3.3V	GPI	Touch sensor Bright Down Control	BRIGHT_DOWN
GPIO6	I/O	3.3V	GPI	Control Bluetooth Switch button	BT_KEY
GPIO7	I/O	3.3V	GPI	Thermal shutdown request	OVERT
GPIO11	I/O	3VSB	GPO	Touch sensor Lcd_on/off Control	LCD_OFF
GPIO34	I/O	3.3V	GPI	Connect to GPI of south bridge	CLR_COMS
GPIO35	I/O	3.3V	GPO	Control Inverter on/ff	LCD_SW

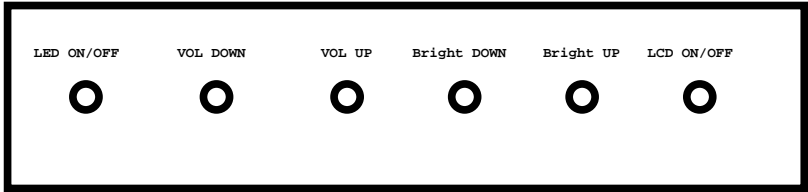
IT8721 GPIO

Signal Name	Type	Voltage	Default	Functional Description	Net name
GP10	I/O	5VSB	GPI	For TOP,LEFT,RIGHT LED Control	LED_BOARD
GP14	I/O	5V	GPI	For BUZZER Control	WT_BEEP
GP17	I/O	3.3V	GPI	For Touch Sensor S3	TOUCH_GPIO
GP20	I/O	3.3V	GPI	LCD_PANEL Straping	PANEL1
GP21	I/O	3.3V	GPI	LCD_PANEL Straping	PANEL2
GP22	I/O	5VDUAL	GPI	Power LED Control	A_GP22
GP23	I/O	5VDUAL	GPI	Power LED Control	A_GP23
GP27	I/O	5V	GPI	MXM module present detect	MXM_PRSENT
GP30	I/O	5V	GPI	Disables RF portion of the MiniCard	WLAN_DIS-
GP34	I/O	3.3V	GPI	Power sequencing sideband	PWR_GOOD
GP35	I/O	5V	GPI	Blue tooth Control	BT_GPIO
GP40	I/O	5VSB	GPI	DIMM DUAL Control	GPIO40_S4S5
GP63	I/O	3.3V	GPI	I/O_SELECT Straping	GPIO63
GP64	I/O	3.3V	GPI	I/O_SELECT Straping	GPIO64

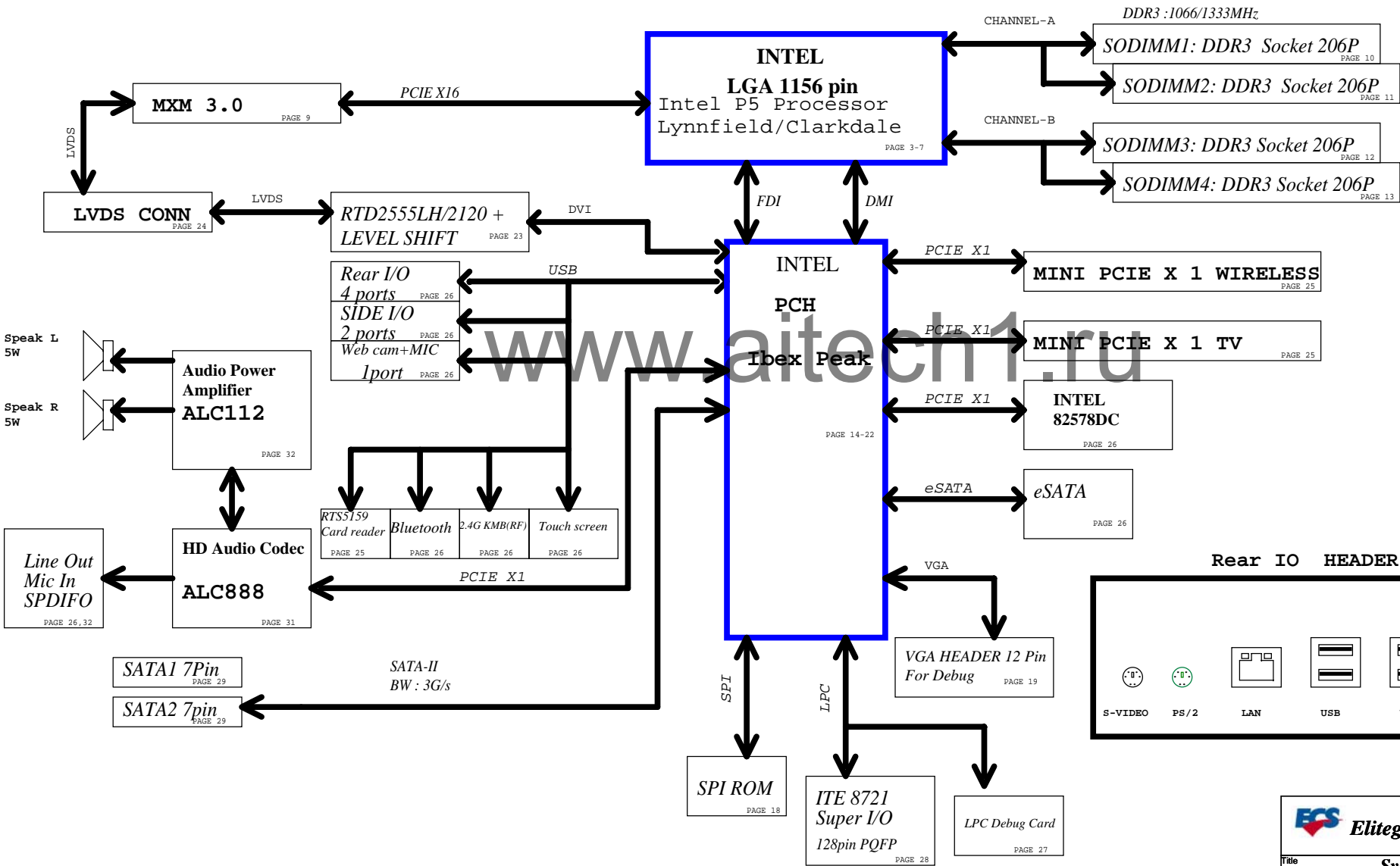
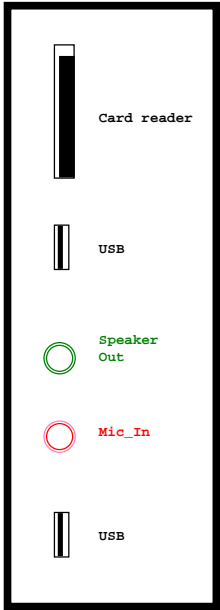
PCB : 251 x 240 ; 6 layers

signal
POWER
signal
signal
GND
signal

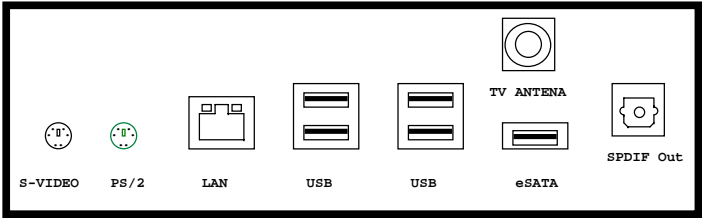
FRONT TOUCH SENSOR



SIDE IO



Rear IO HEADER 64 Pin



**System Block Diagram**

Document Number: **H55H-LAIO**

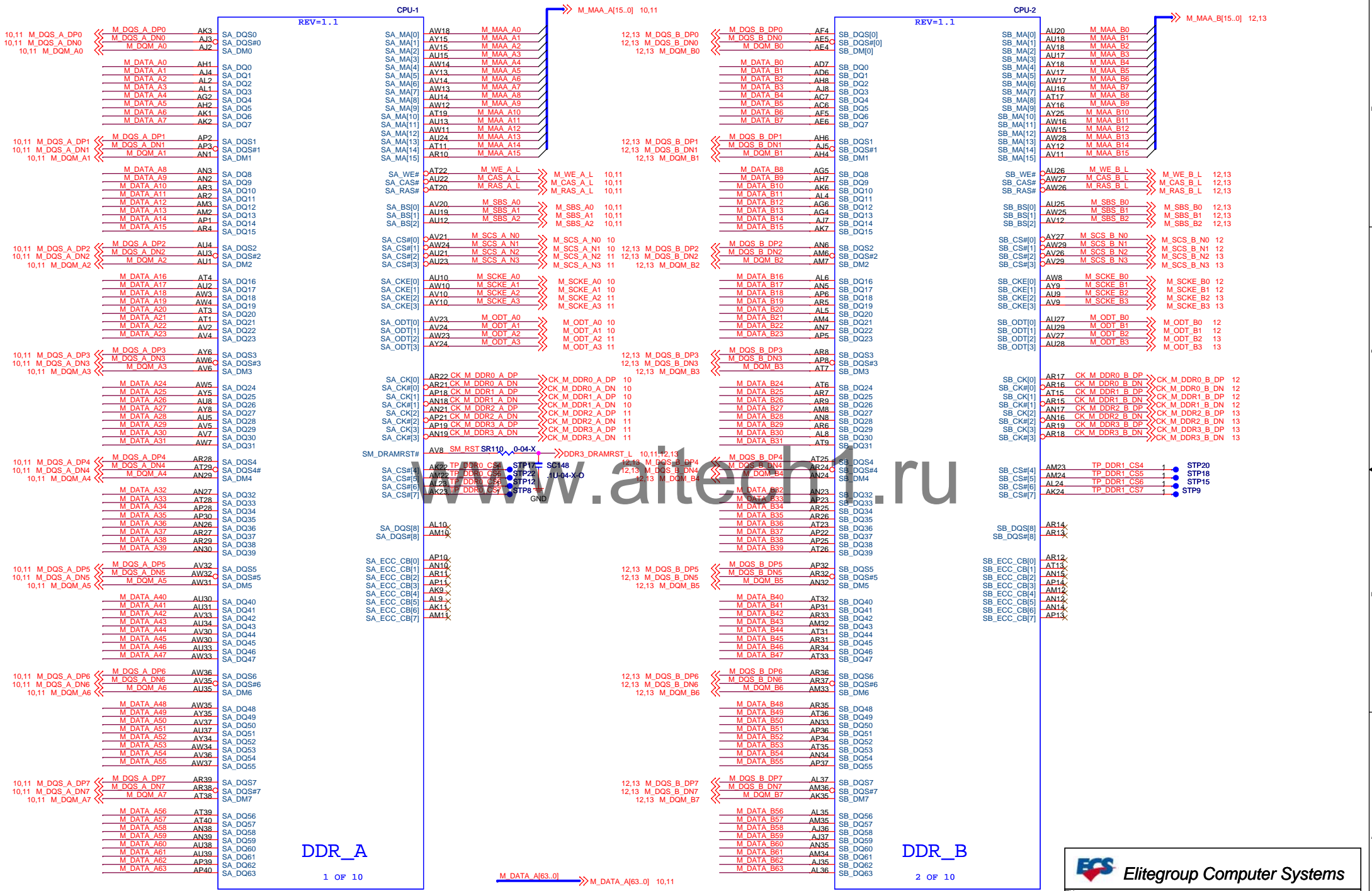
Date: Wednesday, June 09, 2010

Rev 1.0

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DDR\_A

DDR\_B



Elitegroup Computer Systems

Title

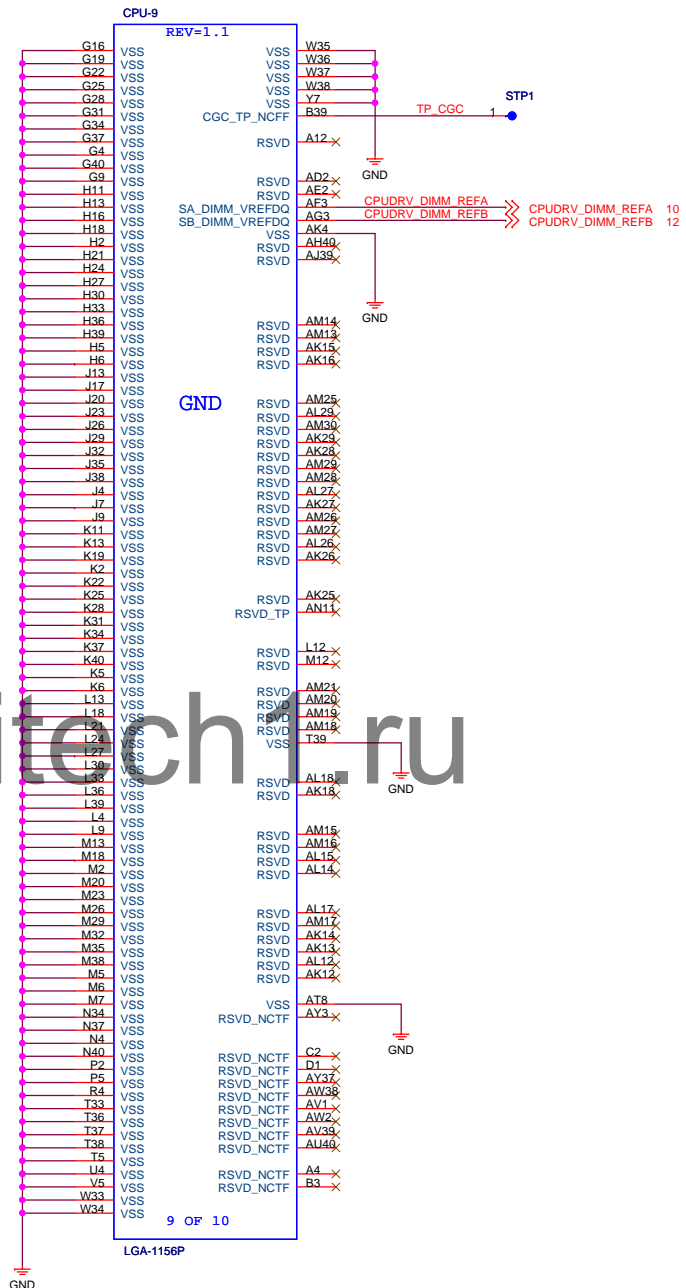
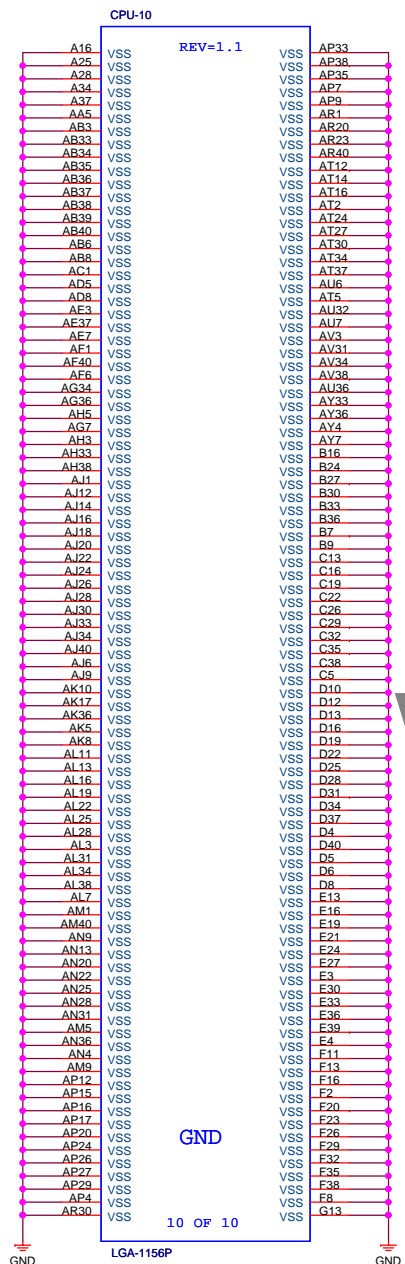
CPU DDR3-A/DDR3-B

Size	Document Number	Rev
Custom	H55H-LAIO	1.0

Date:	Wednesday, June 09, 2010	Sheet	5	of	41
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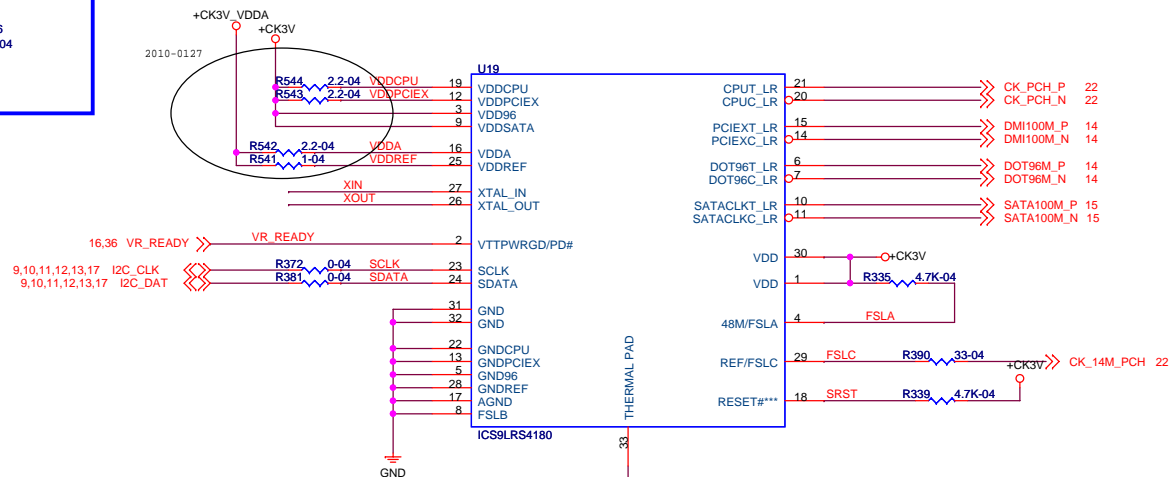
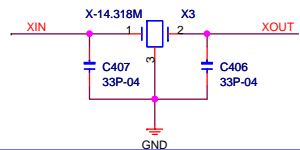






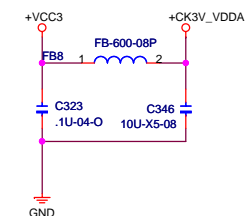
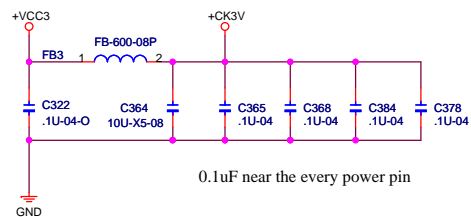
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The C206/C207 value depend on CL of X2 crystal  
if CL=20pF C206/C207=33pF  
if CL=32pF C206/C207=56pF

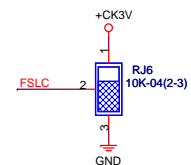
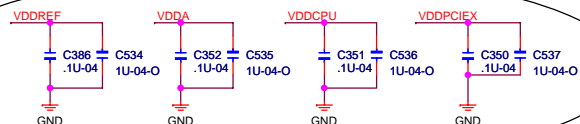


BOTTOM PAD  
CONNECT TO GND  
Through 1 VIAs

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2010-0203



Functionality Table FSLC,FSLA = 01, CPU\_CLK = 133MHZ

Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU MHZ	PCIEX MHZ	SATA MHZ	DOT96 MHZ
0	0	1	133.33	100.00	100.00	96.00
1	0	1	100.00	100.00	100.00	96.00

CPU PLL Spread Frequency Selection Table

FSLC B0b2	FSLB B0b1	FSLA B0b0	CPU MHZ	Spread% B0b5=1
0	0	1	133.33	0.5% Down
1	0	1	100.00	0.5% Down

PCIEX PLL Spread Frequency Selection Table

B19b4	B19b3	FSLC B0b2	FSLB B0b1	FSLA B0b0	PCIEX MHZ	Spread %
0	0	0	0	1	100.00	0.5% Down
0	0	1	0	1	100.00	0.5% Down
1	0	0	0	1	100.00	NO Spread
1	0	1	0	1	100.00	NO Spread



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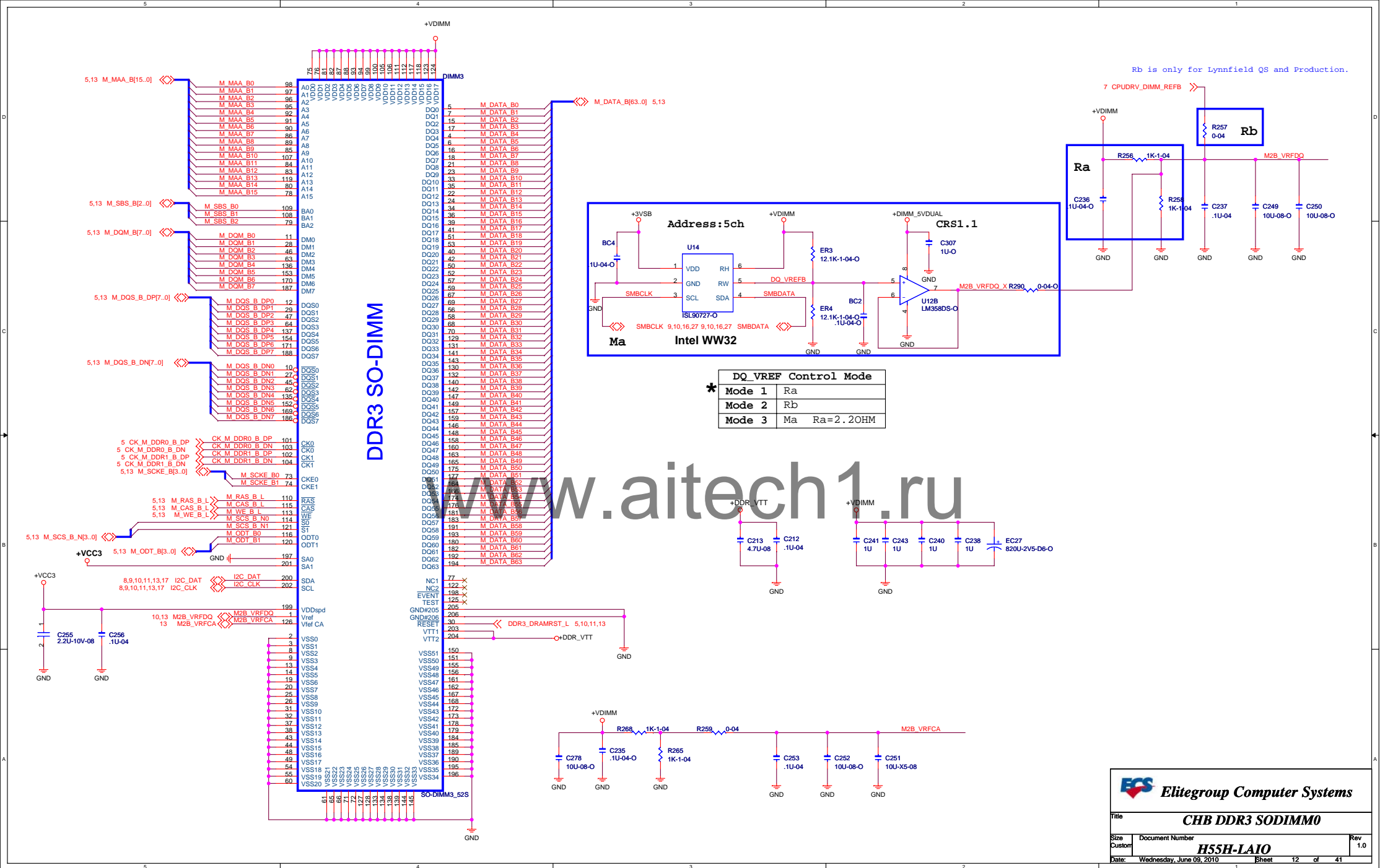
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Size	Document Number	H55H-LA10	
Custom			Rev 1.0
Date:	Wednesday, June 09, 2010	Sheet 8	of 41







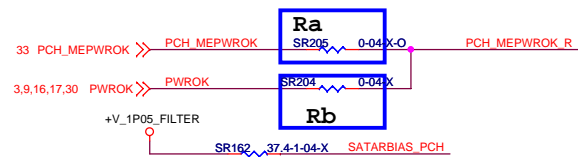




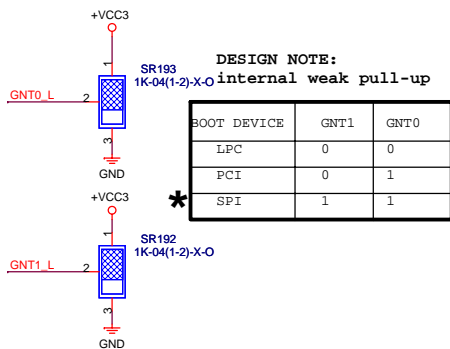
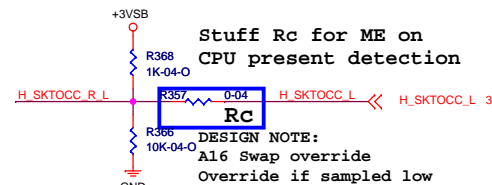
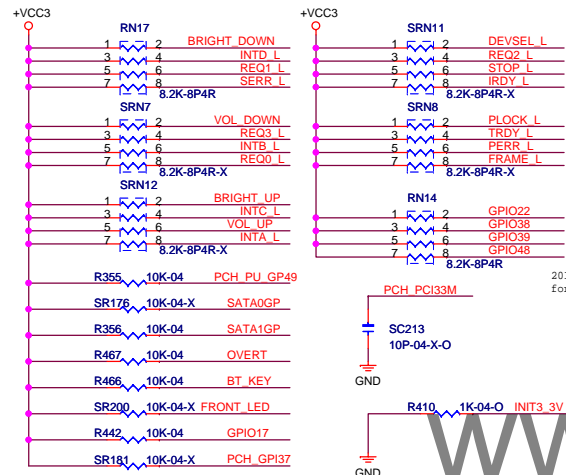






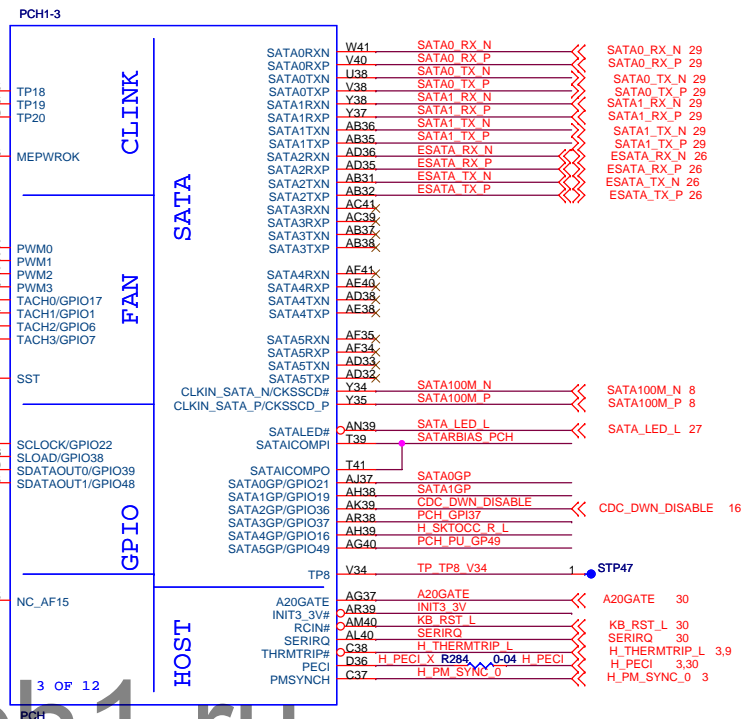
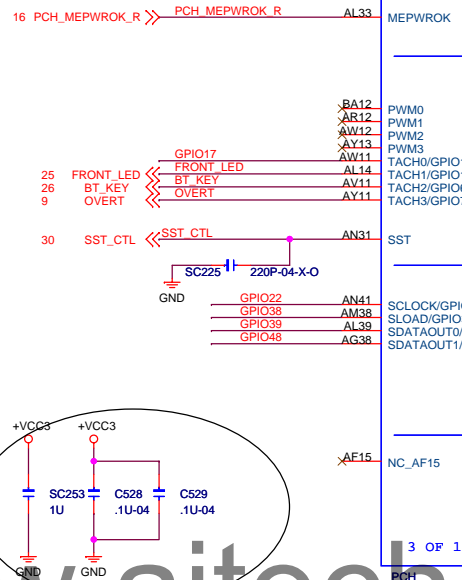


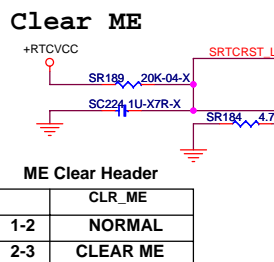
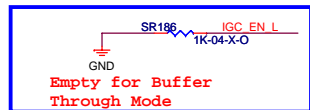
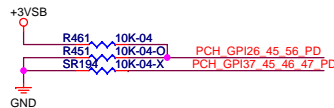
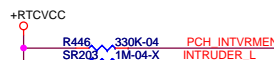
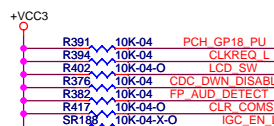
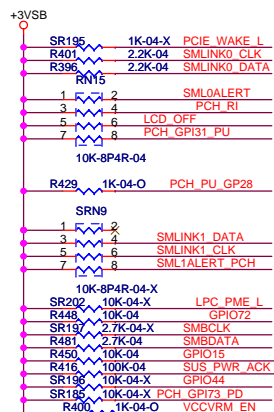
ME_PWROK	
AMT	Ra
Non-AMT	Rb



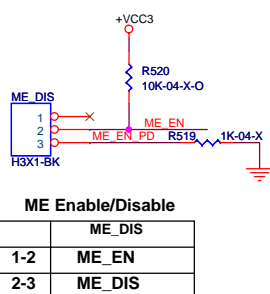
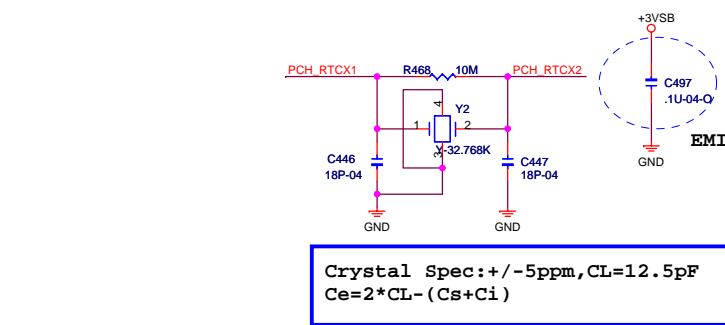
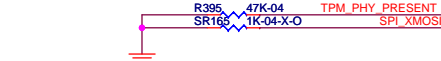
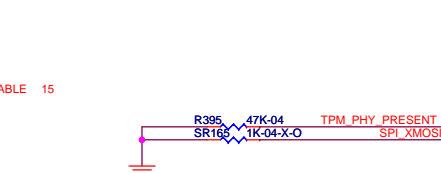
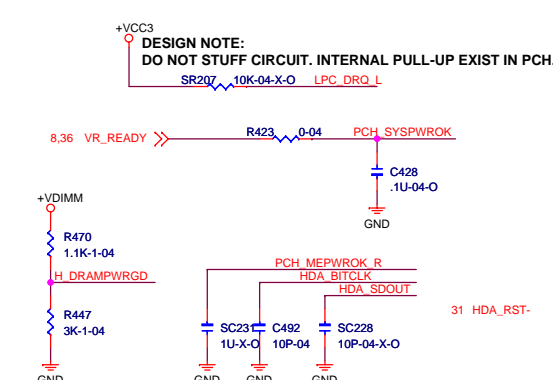
DESIGN NOTE:  
internal weak pull-up

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

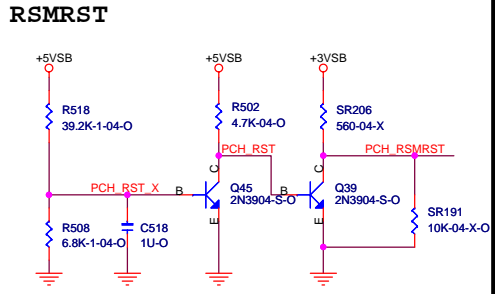




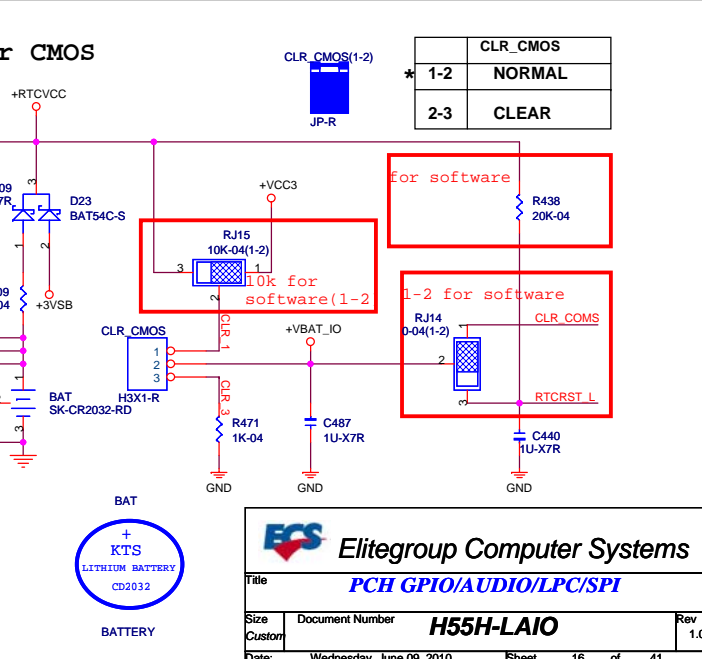
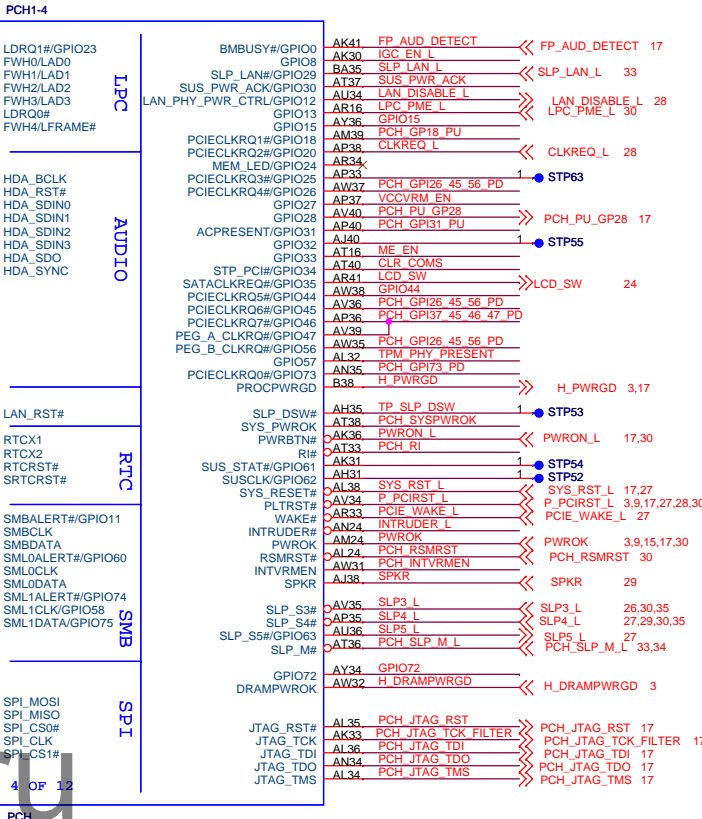
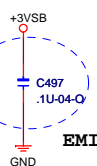
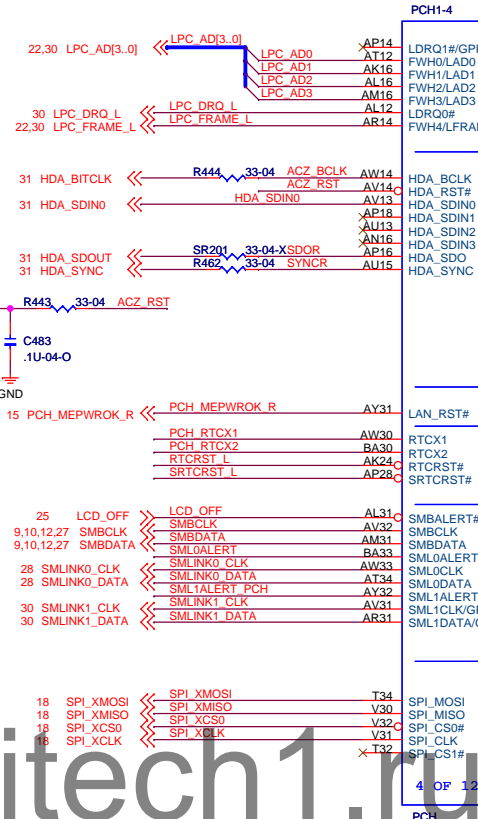
ME Clear Header	
1-2	NORMAL
2-3	CLEAR ME



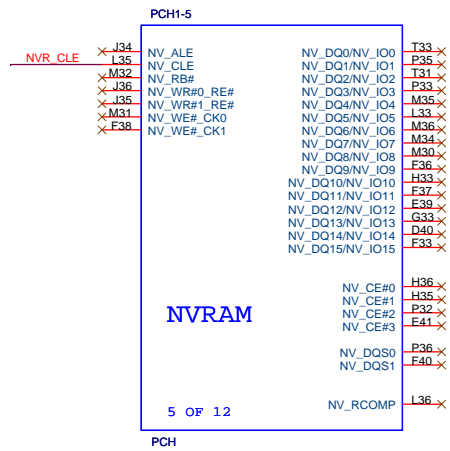
ME Enable/Disable	
1-2	ME_EN
2-3	ME_DIS



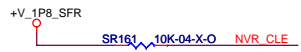
### RSMRST



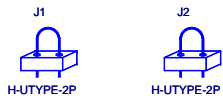
### Clear CMOS



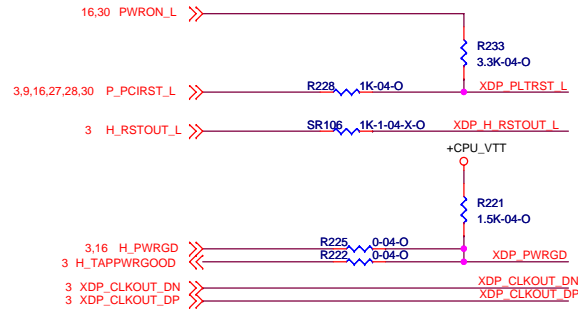
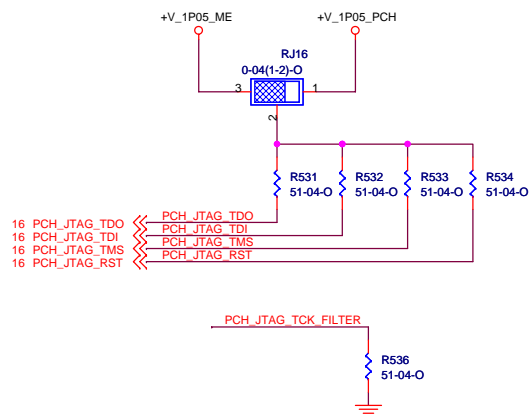
DESIGN NOTE:  
High:Enable Intel AT-d  
Low:Disable Intel AT-d



DESIGN NOTE:  
High:DC Coup TX/RX to VCC  
Low:DMI Termination Voltage



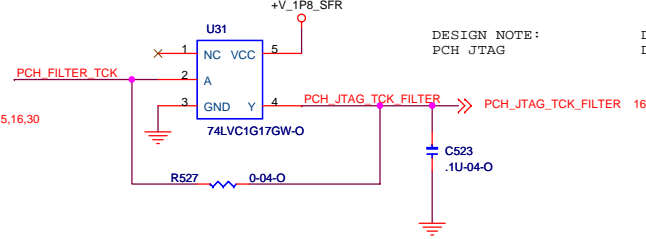
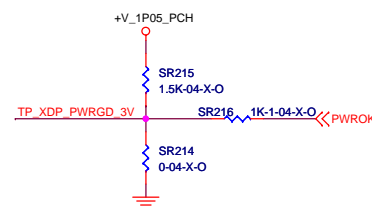
### WW50



CLK Souce:Default use PCH

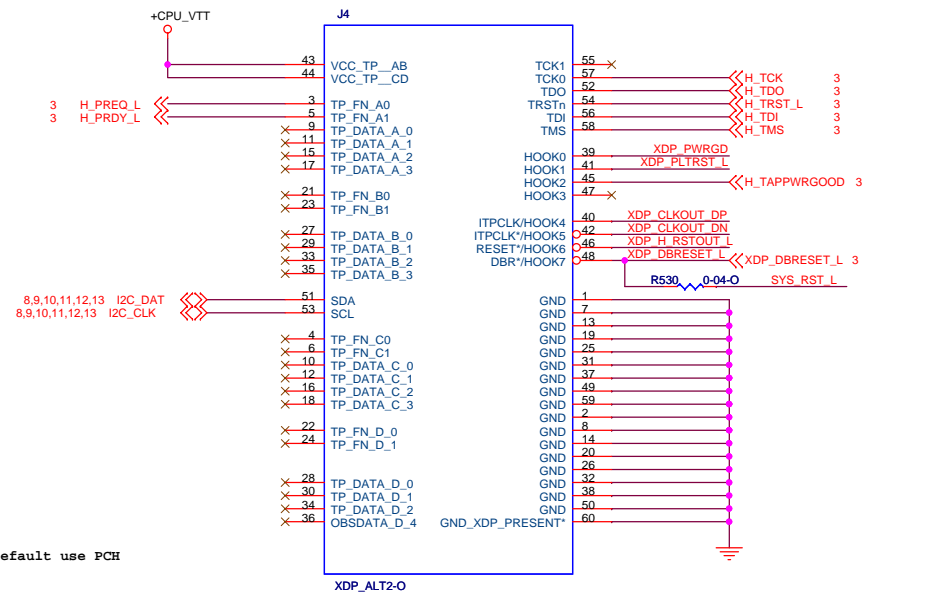


PCH PIN	RefDes	ES1	ES2	Production Systems
TDO	R110	No Stuff	100 Ohms	51 Ohms
TMS	R113	100 Ohms	100 Ohms	51 Ohms
TDI	R109	100 Ohms	100 Ohms	51 Ohms
TRST#	R112	10K Ohms	10K Ohms	51 Ohms
	RJ6	0(2-3)	0(2-3)	0(1-2)

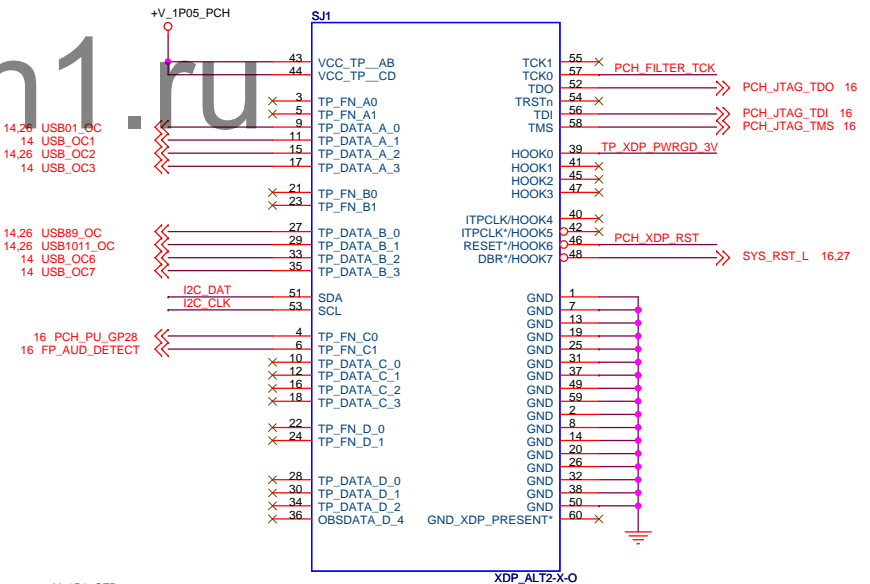


DESIGN NOTE:  
PCH JTAG

DESIGN NOTE:  
DEFENSIVE DESIGN



DESIGN NOTE:  
DEFAULT EMPTY SITE ON PAGE 94: XDP\_PWRGD RES (R108PR) TO VTT\_OUT\_RIGHT  
DEFAULT EMPTY SITE ON PAGE 123: XDP\_PWRGD RES (R3S3EV) TO V\_FSB\_VTT  
DEFAULT STUFF SITE: (R662EV) TO TP\_XDP\_PWRGD

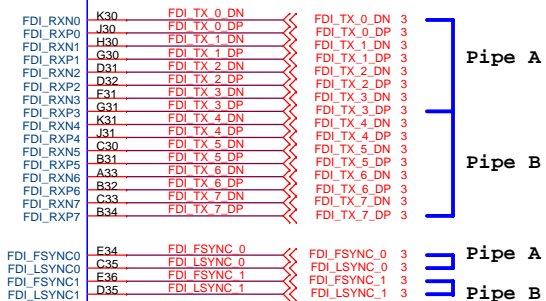


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## PCH FDI Link

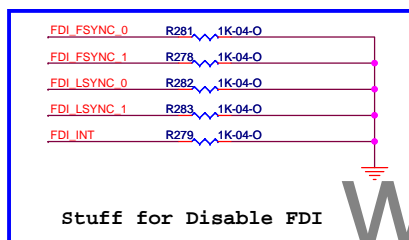
PCH1-7

### FDILINK

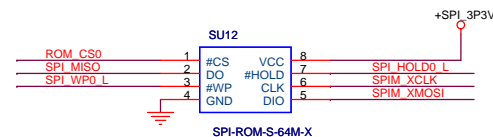
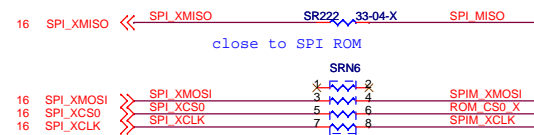


7 OF 12 FDI\_INT B36 FDI\_INT FDI\_INT 3

PCH



## SPI ROM

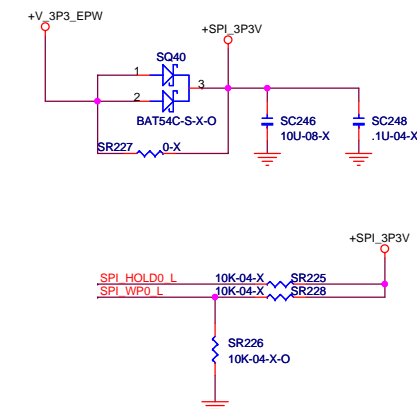


SMD TYPE

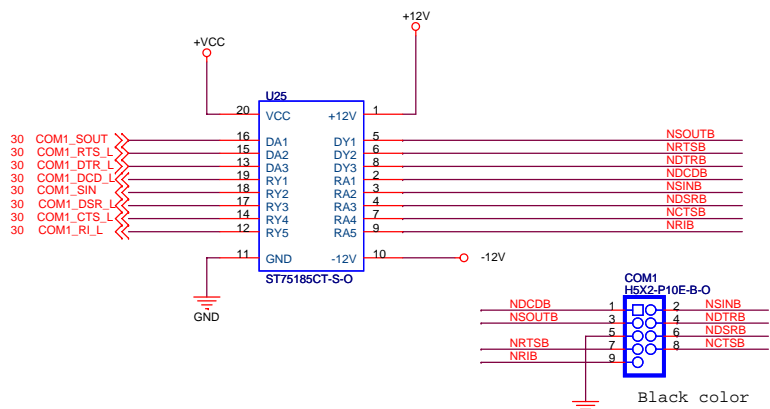
SPI\_DEBUG(1-3)



JP-R

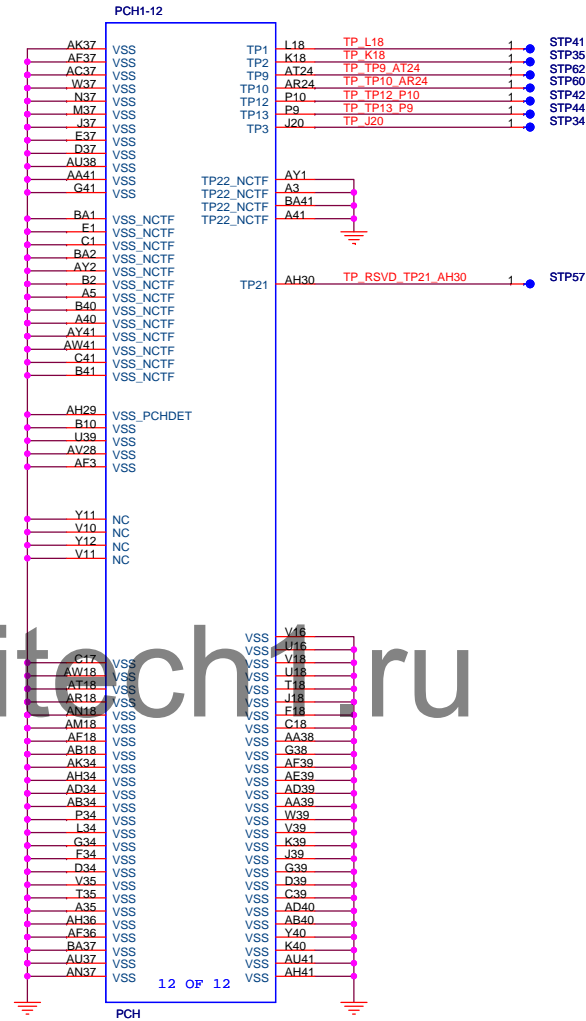
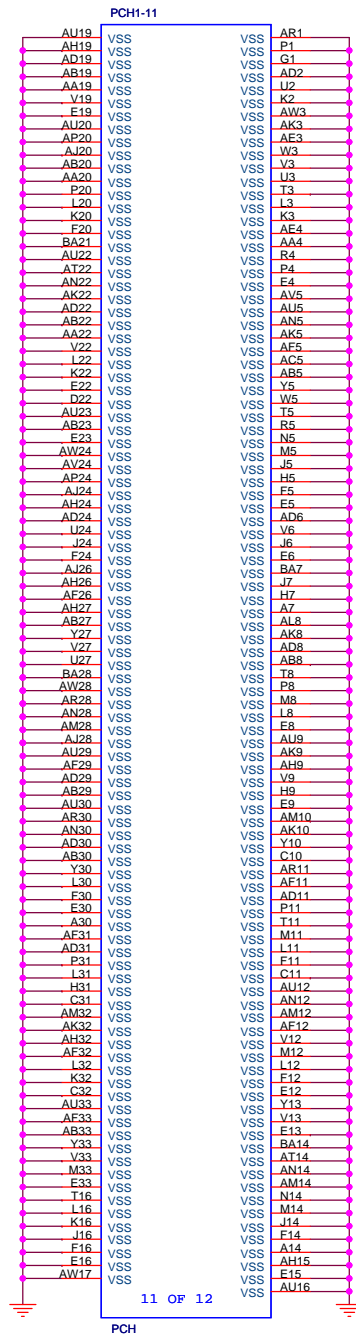


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Reserved Debug



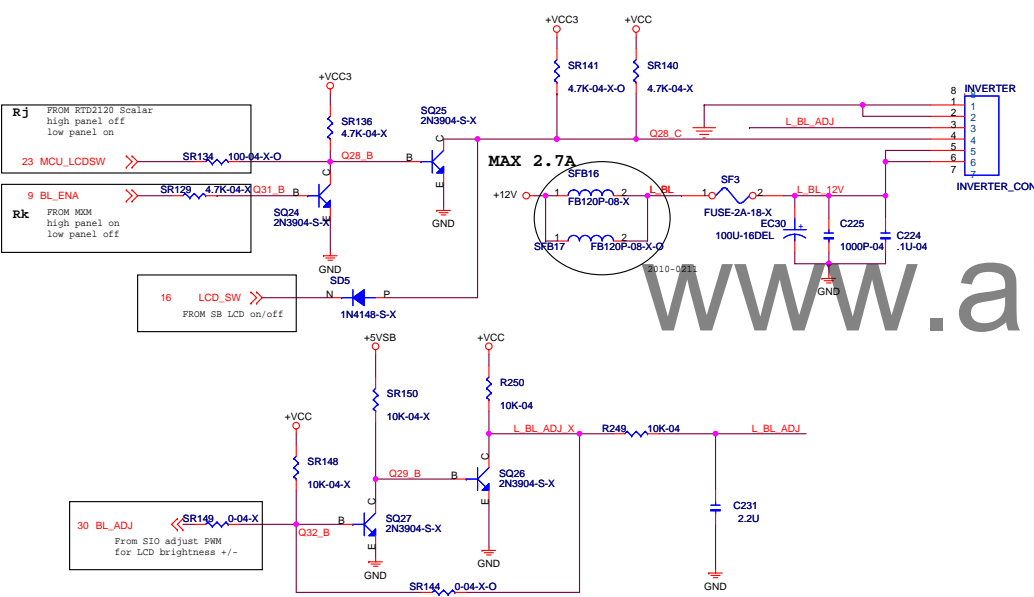
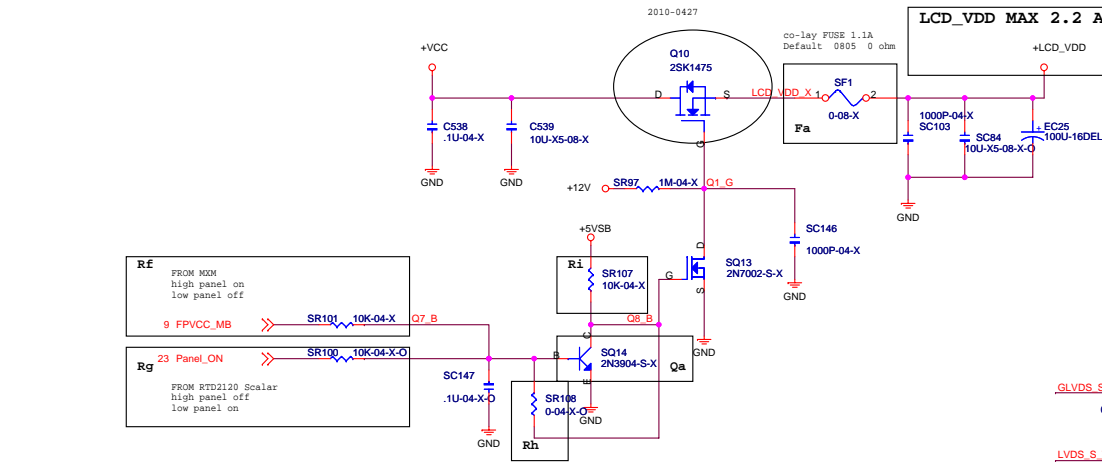






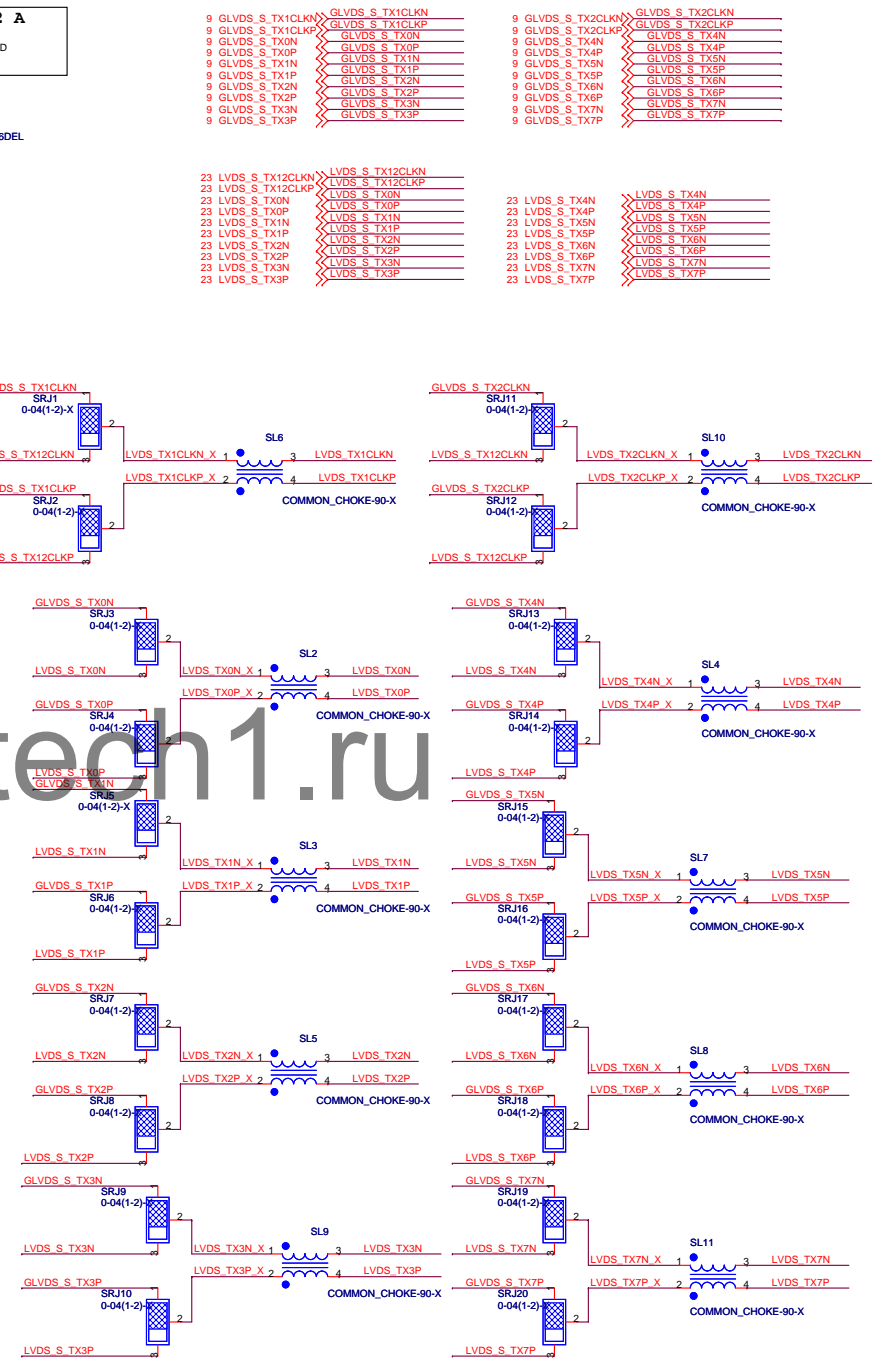
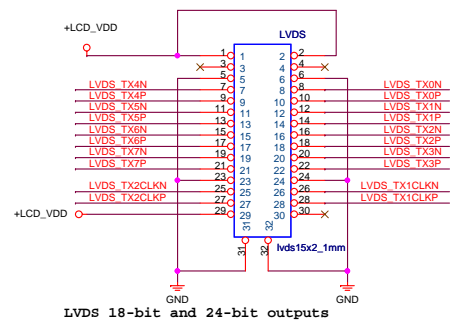


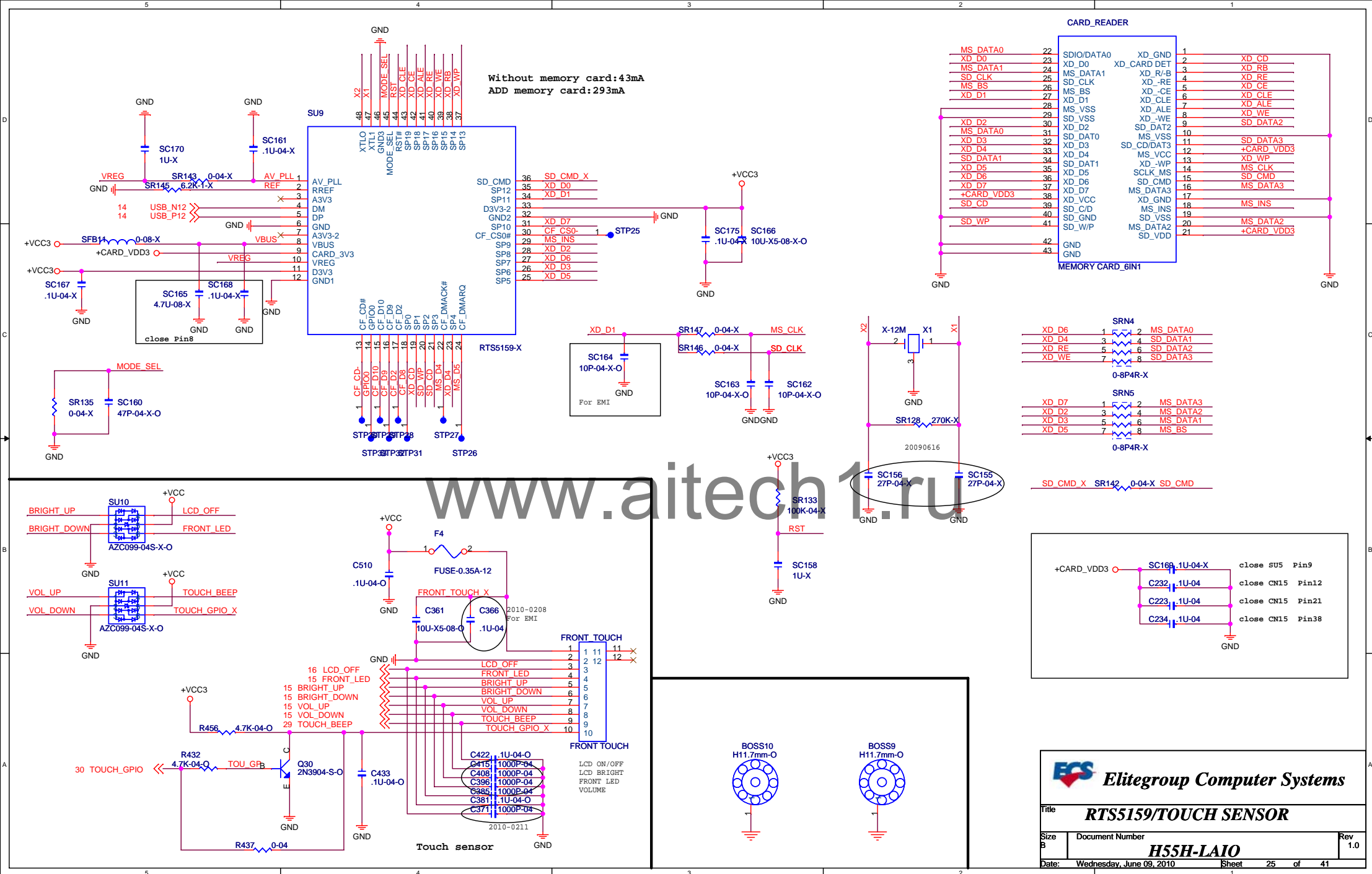


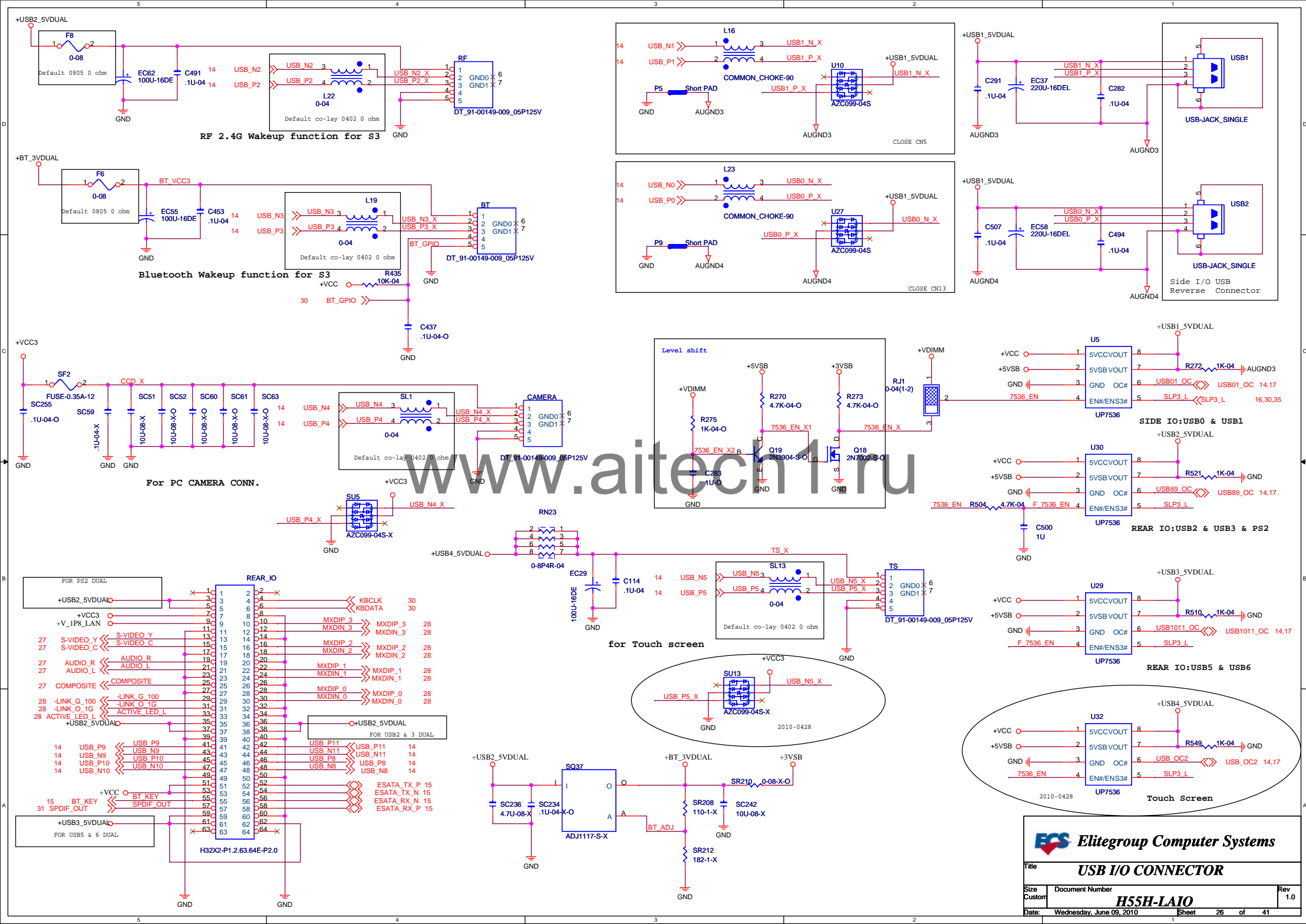


**LVDS BOM Difference**

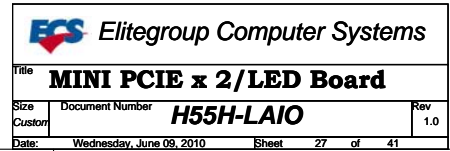
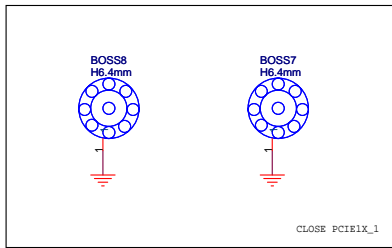
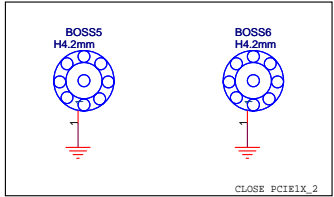
Location	MXM 3.0	SCALER
Rf	V	X
Rg	X	V
Rh	X	V
Ri	V	X
Rj	X	V
Rk	V	X
Qa	V	X
Fa	Default 0805 0 ohm	Default 0805 0 ohm



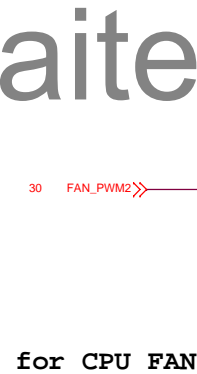
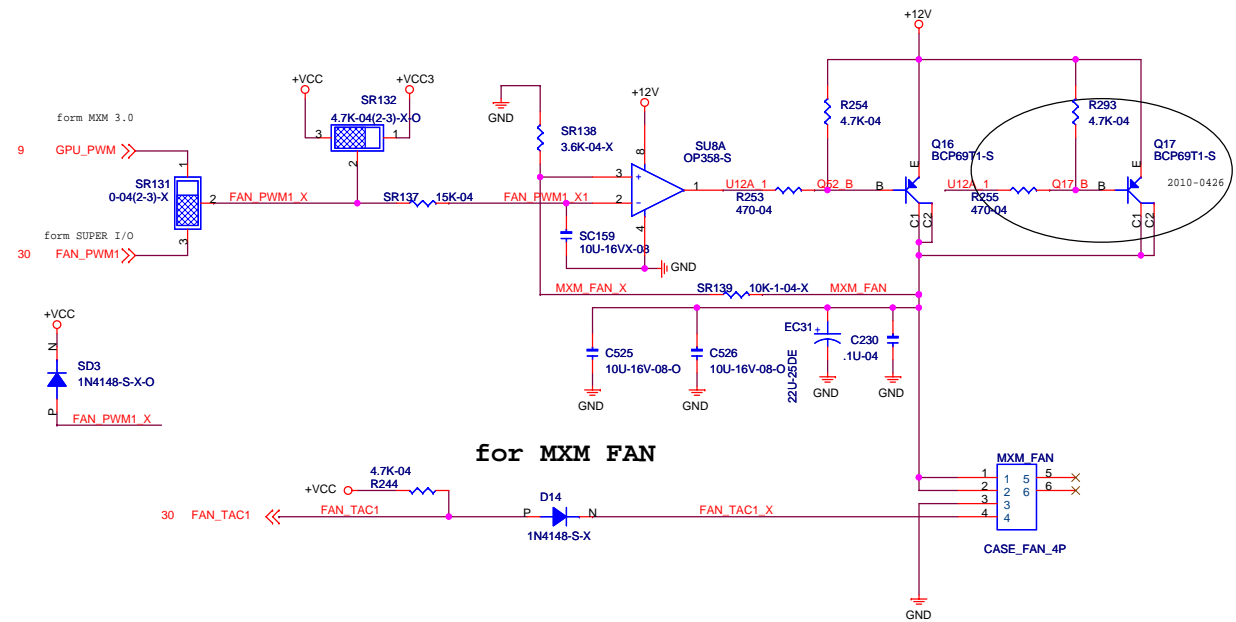
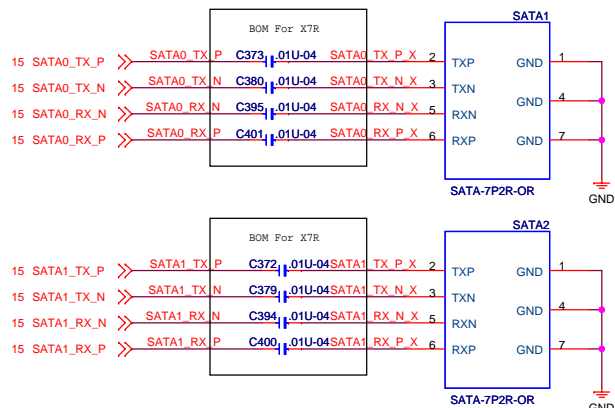
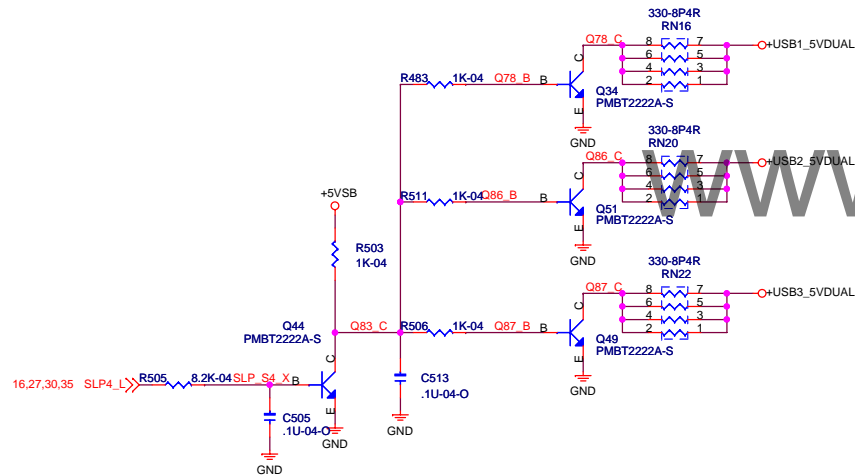
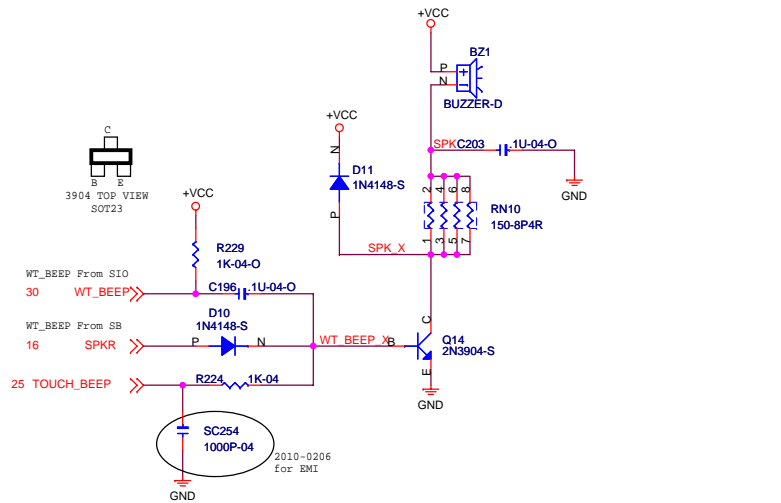


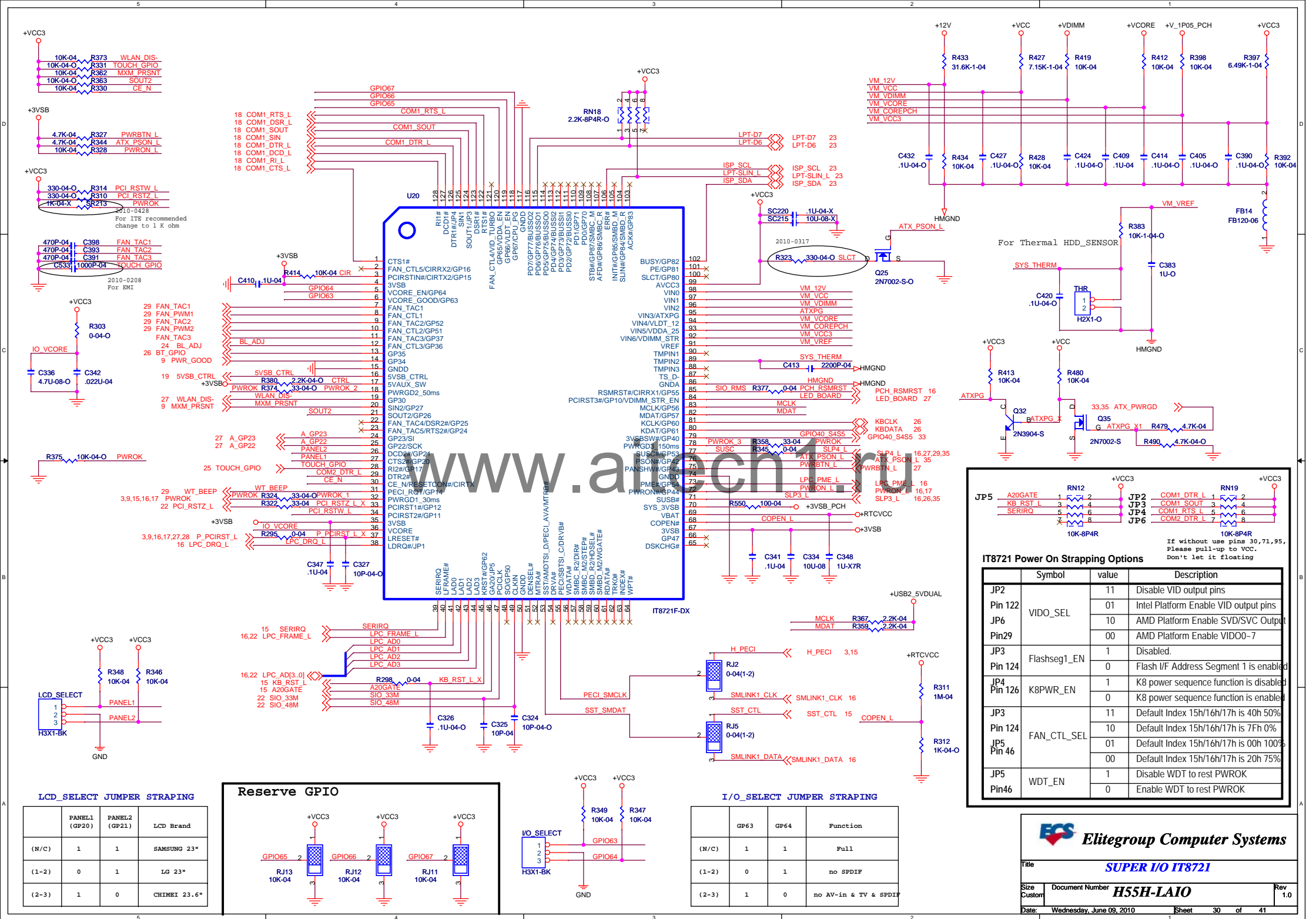


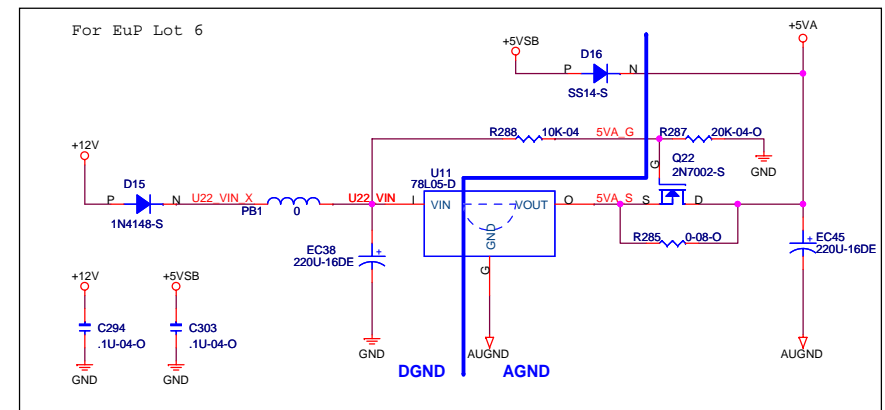


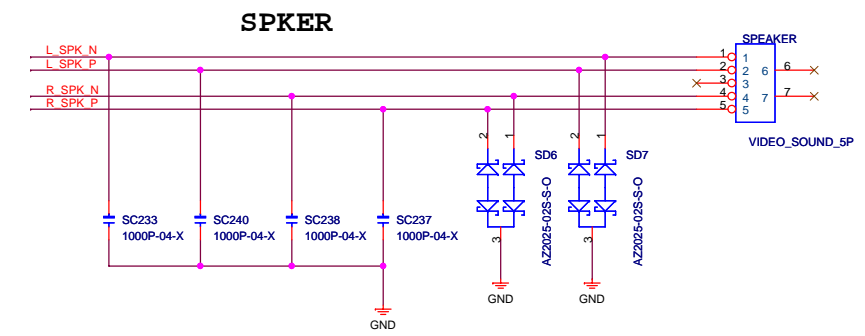
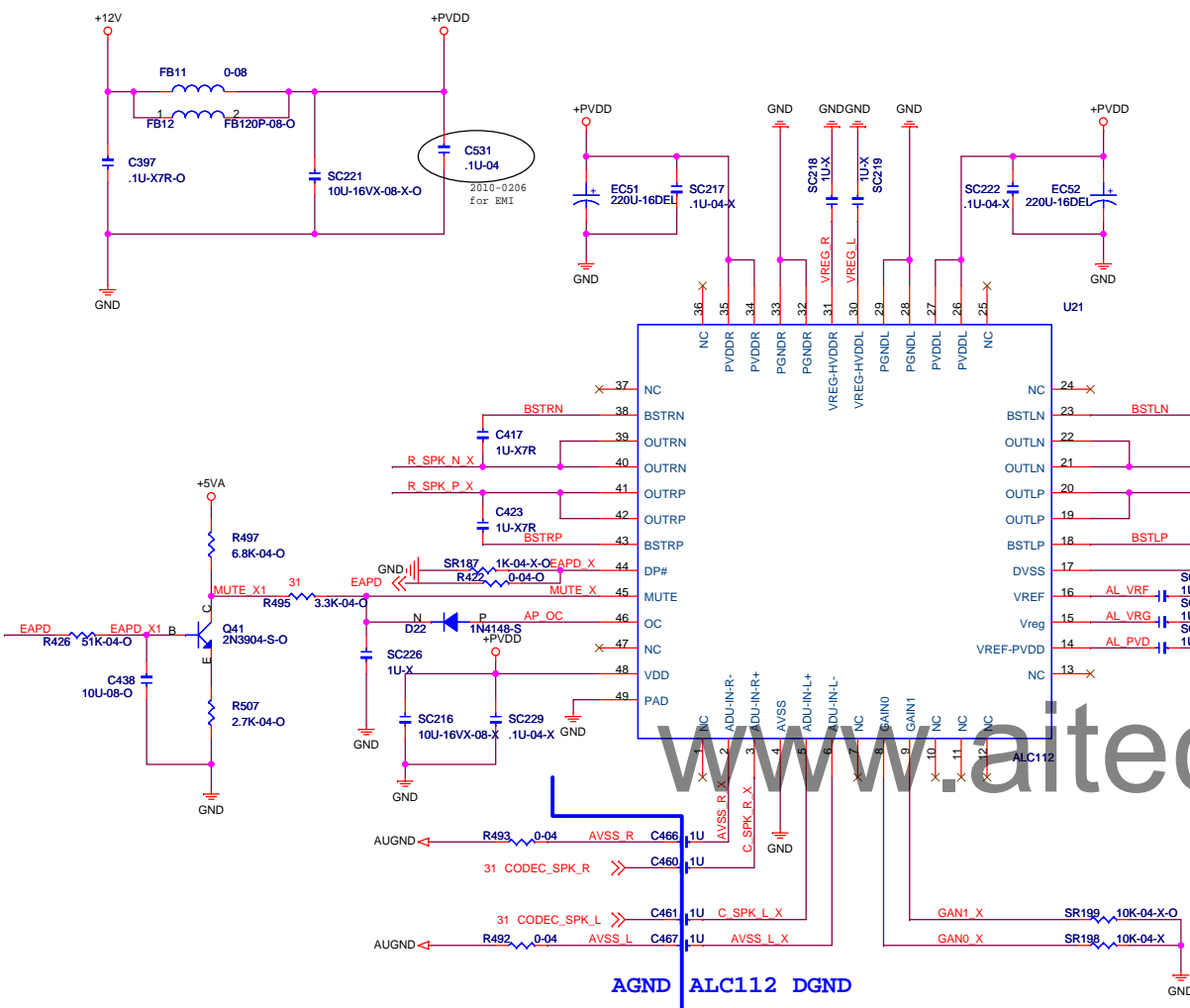






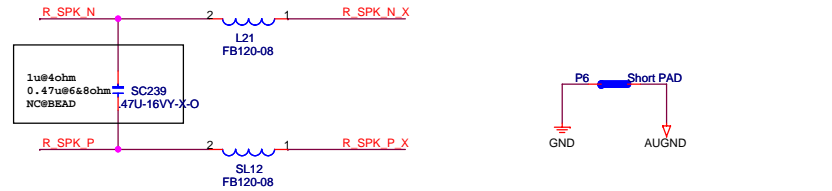
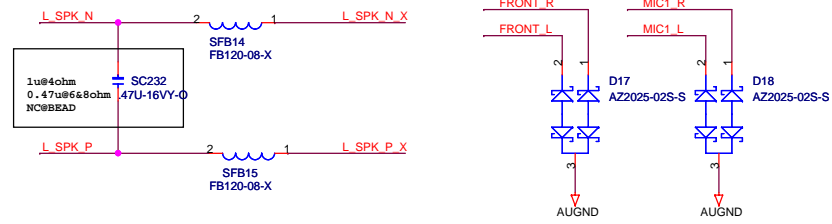
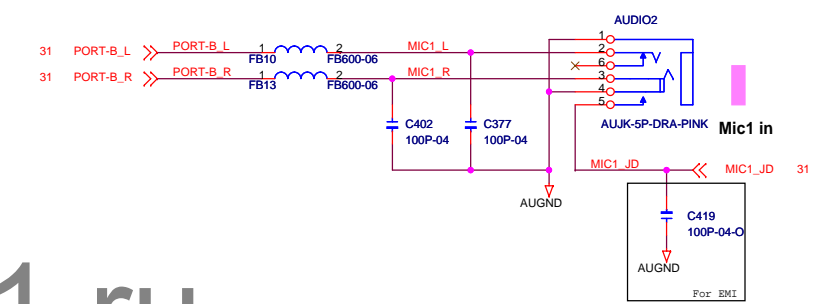
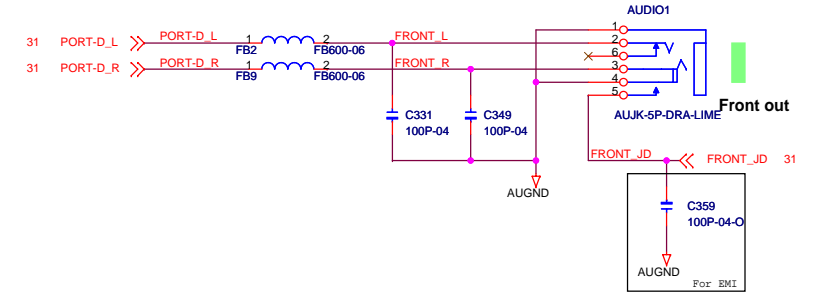




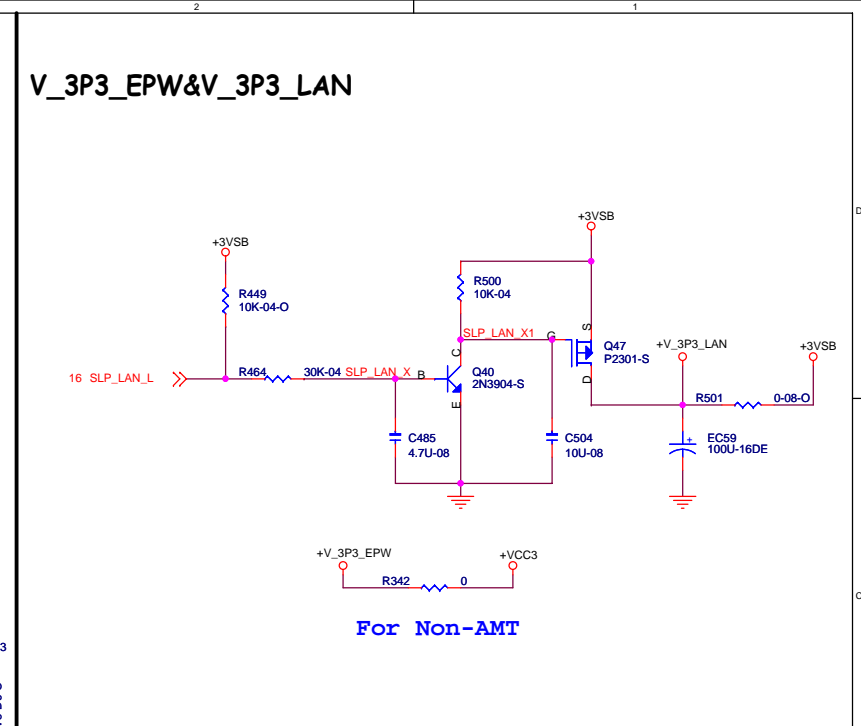


Internal PU w/z 40K ohm

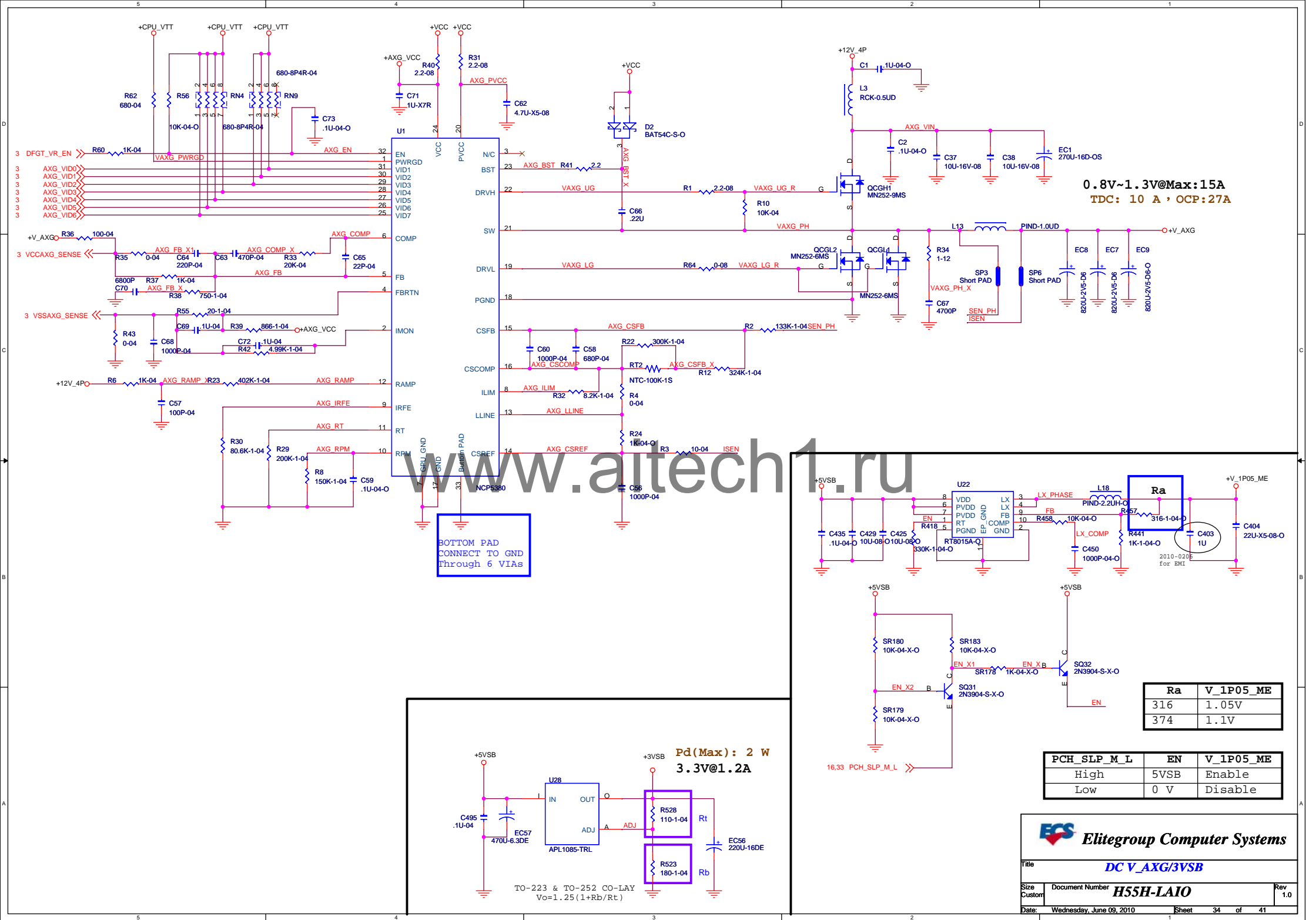
Gain 1	Gain 0	Boost Gain
0	0	6 dB
0	1	12 dB
1	0	18 dB
1	1	24 dB

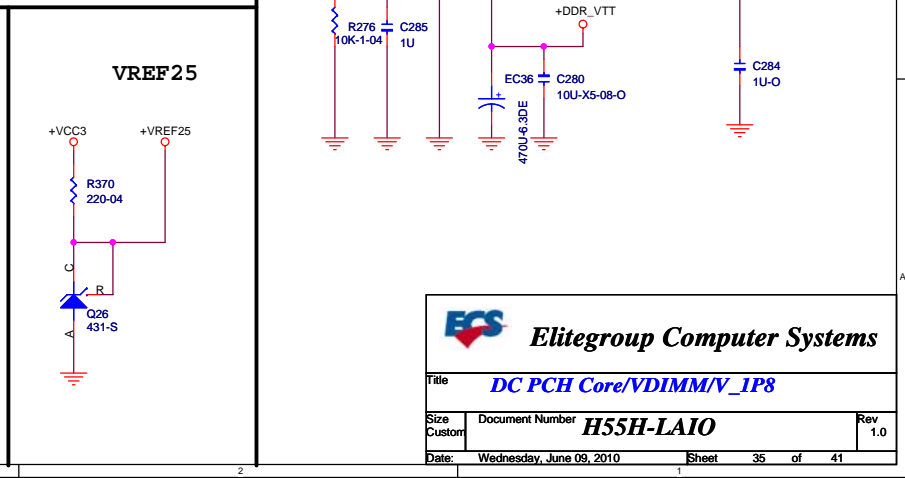
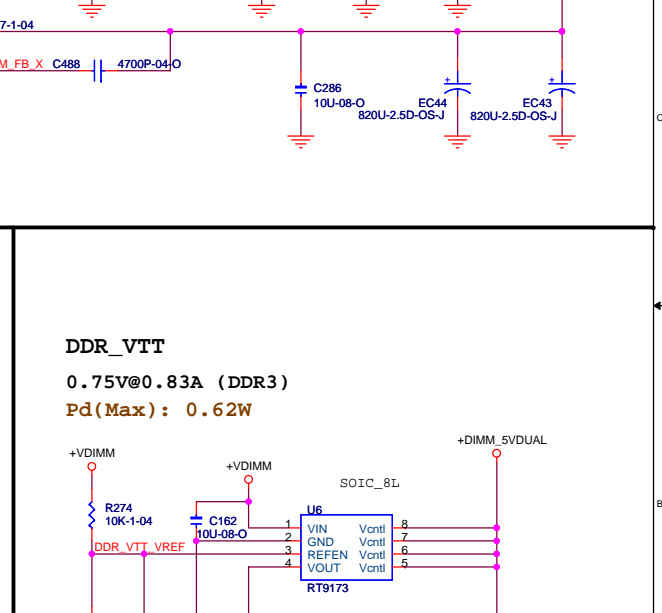
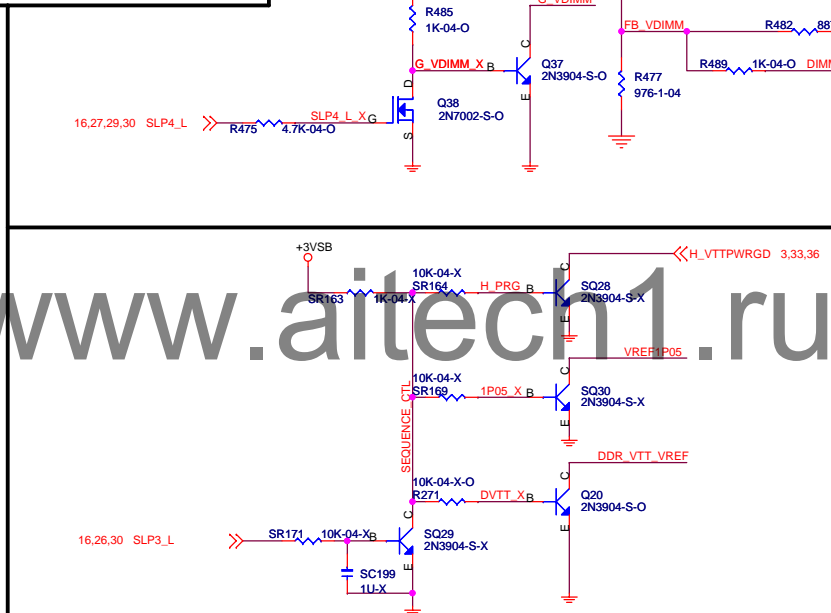
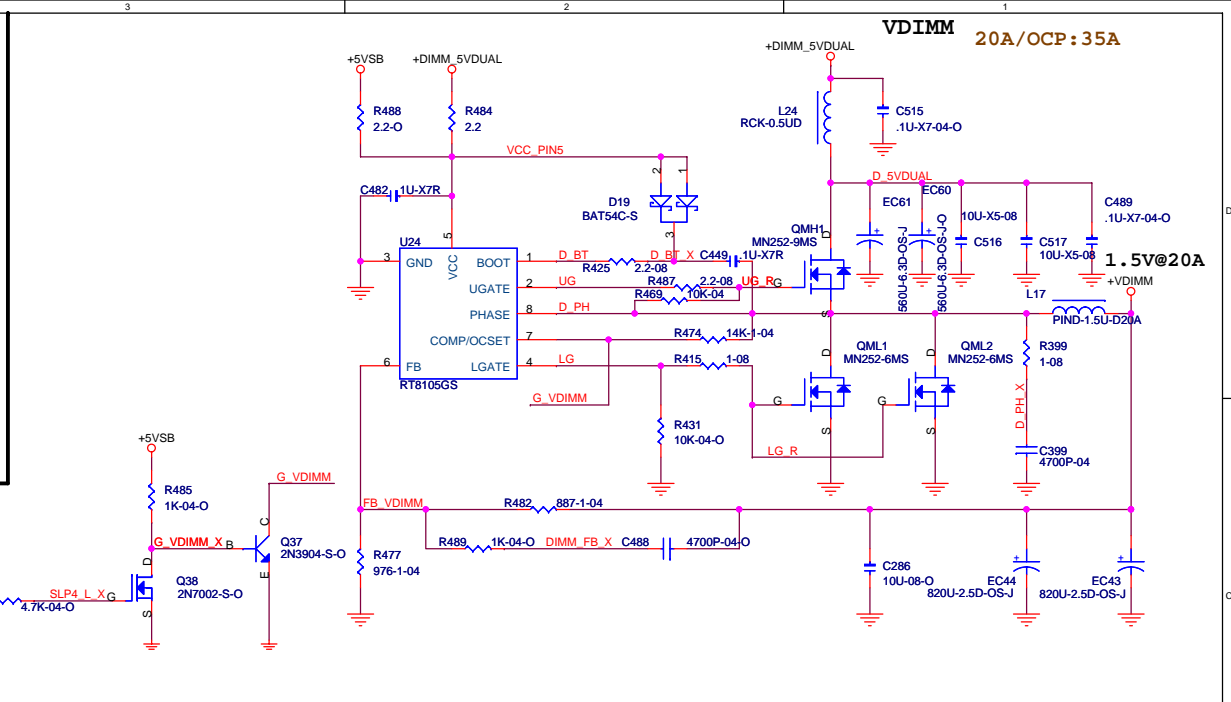


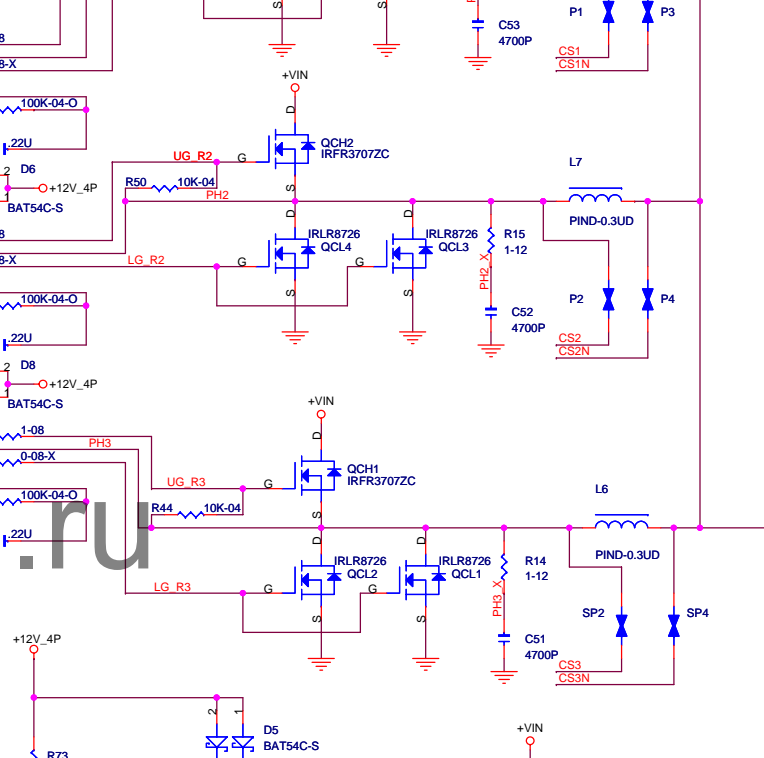
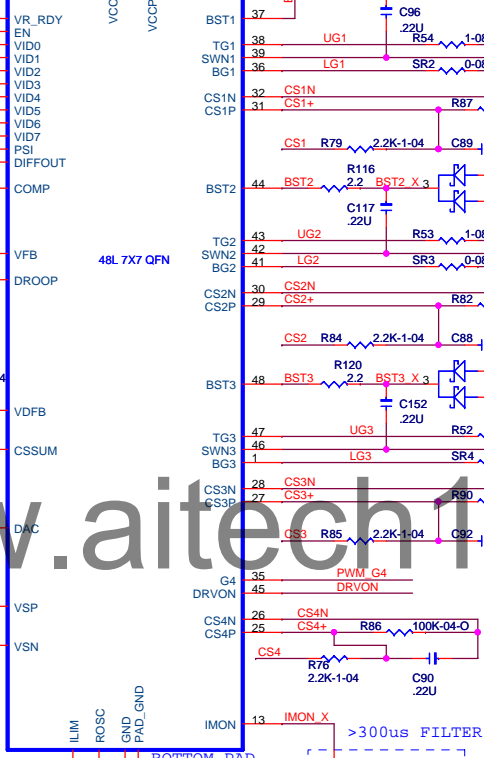
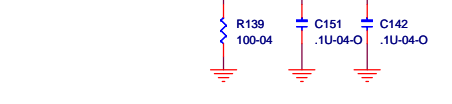
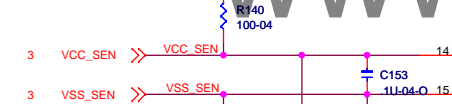
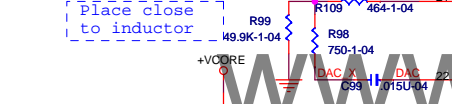
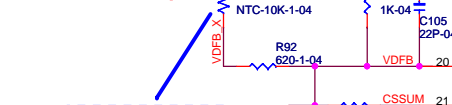
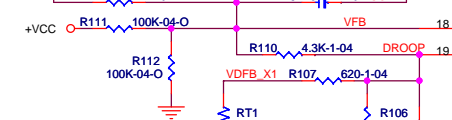
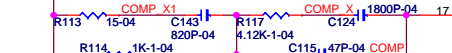
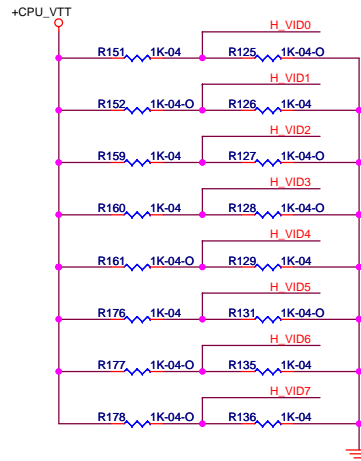
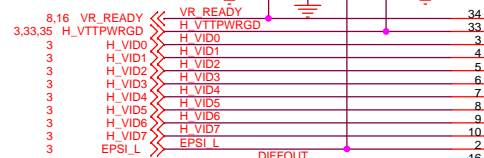




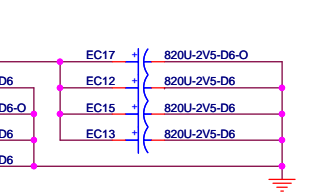
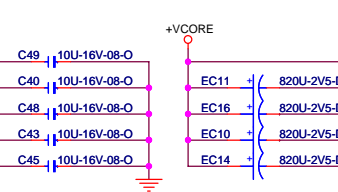
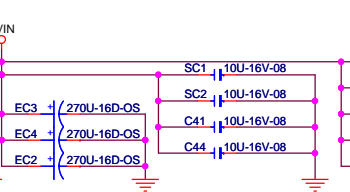
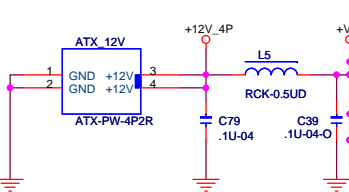
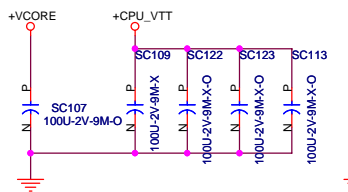
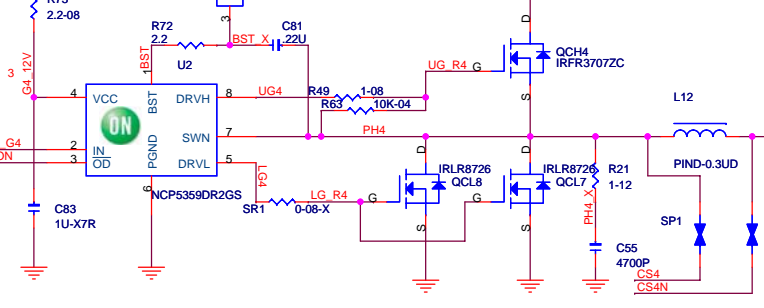
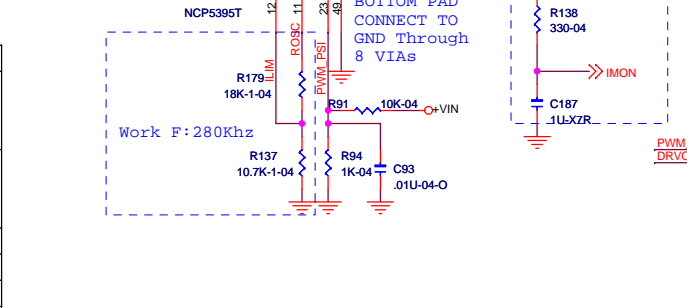
VTT_SEL		CPU Type
H	1.05V	
L	1.1V	Hav/lynn

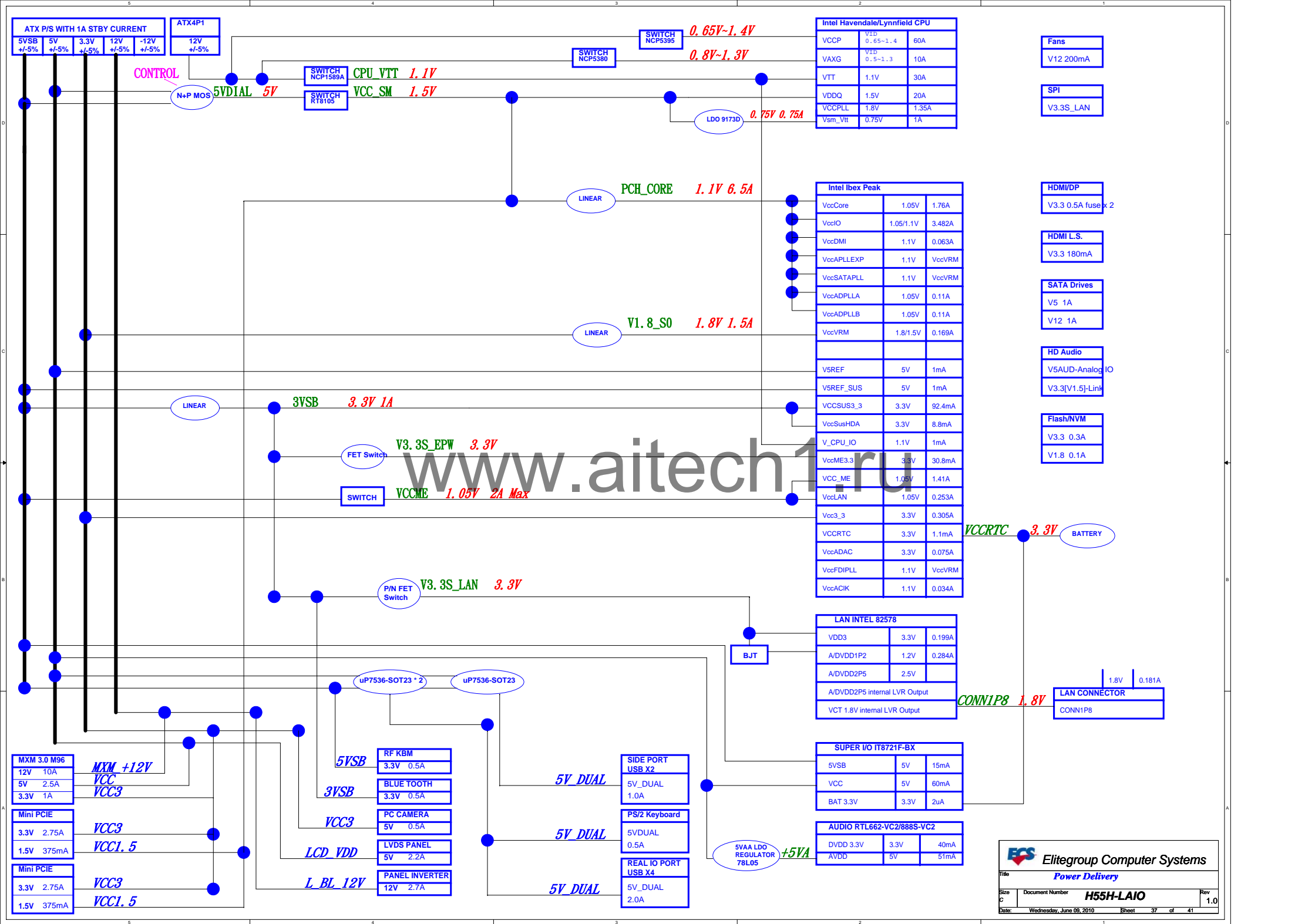




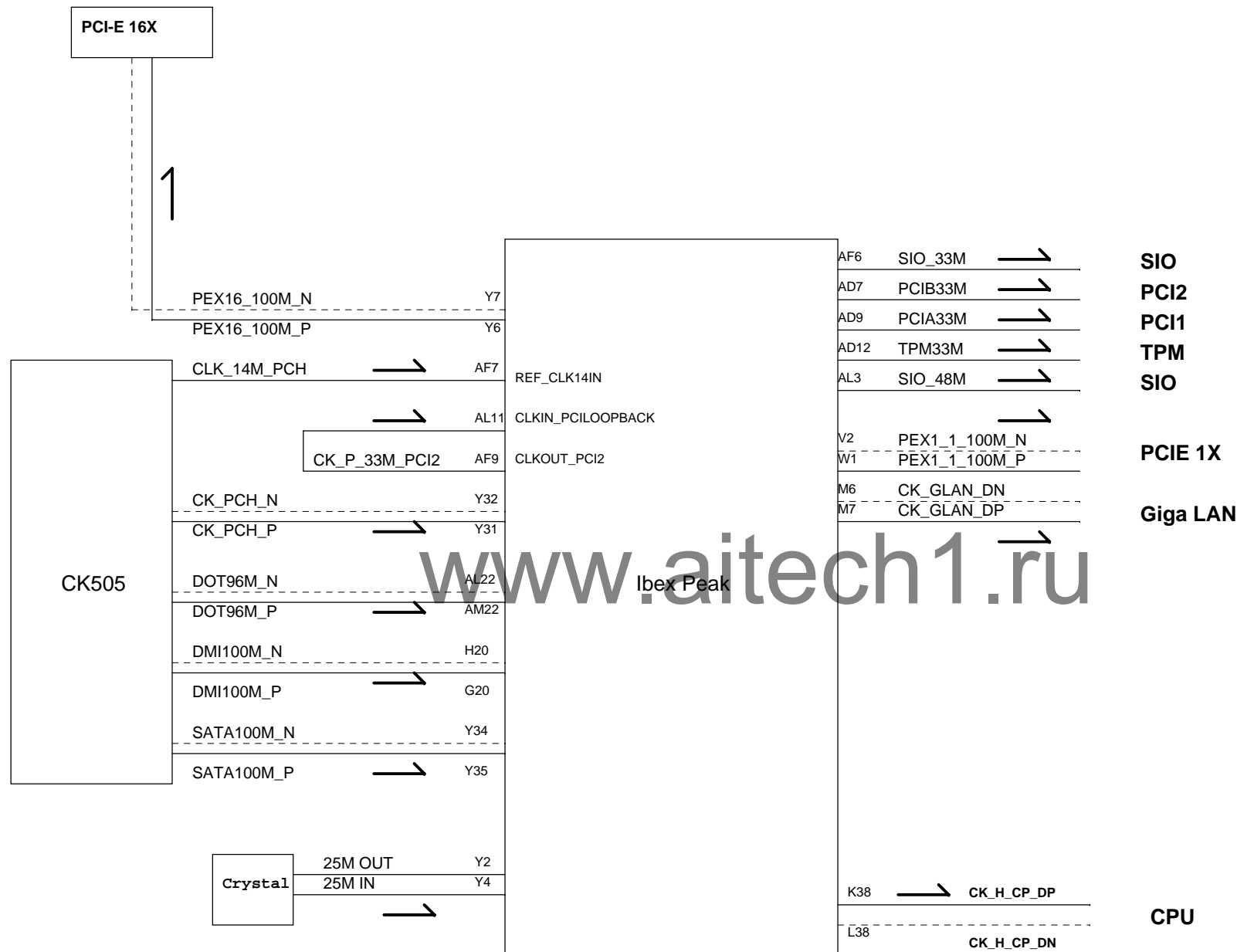


	FUNCTION	Setting	Clarkdale	Lynnfield
VID0	MIS0	1	Support (09A)	Support (09A)
VID1	MIS1	0		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	lcc(MAX)=120A	lcc(MAX)=120A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		











## CPU Strap Function

CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED				REVERSED
3	Static Lane Number Reversal				REVERSED
4	REVERSED				REVERSED
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

POWER ON CONFIGURATION (POC) TABLE

	FUNCTION	Setting	Clarkdale	Lynnfield
VID0	MISO	1	Support (09A)	Support (09A)
VID1	MIS1	0		
VID2	MIS2	1		
VID3	IMON CONFIG0	1		
VID4	IMON CONFIG1	0	lcc(MAX)=120A	lcc(MAX)=120A
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

## PCH Strap Function

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

\*

## IT8721 Strap Function

IT8721 Power On Strapping Options			
	Symbol	value	Description
JP2	VIDO_SEL	11	Disable VID output pins
Pin 122		01	Intel Platform Enable VID output pins
JP6		10	AMD Platform Enable SVD/SVC Output
Pin29		00	AMD Platform Enable VIDO0-7
JP3	Flashseg1_EN	1	Disabled.
Pin 124		0	Flash I/F Address Segment 1 is enabled
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126		0	K8 power sequence function is enabled
JP3	FAN_CTL_SEL	11	Default Index 15h/16h/17h is 40h 50%
Pin 124		10	Default Index 15h/16h/17h is 7Fh 0%
JP5		01	Default Index 15h/16h/17h is 00h 100%
Pin 46		00	Default Index 15h/16h/17h is 20h 75%
JP5	WDT_EN	1	Disable WDT to rest PWROK
Pin46		0	Enable WDT to rest PWROK

If without use pins 30,71,95,  
Please pull-up to VCC.  
Don't let it floating

## Clock(ICS9LRS4180) Strap Function

Functionality Table FSLC,FSLA = 01, CPU\_CLK = 133MHz

Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU MHZ	PCIEX MHZ	SATA MHZ	DOT96 MHZ
0	0	1	133.33	100.00	100.00	96.00
1	0	1	100.00	100.00	100.00	96.00

PCIEX PLL Spread Frequency Selection Table

B19b4	B19b3	FSLC B0b2	FSLB B0b1	FSLA B0b0	PCIEX	Spread
					MHZ	%
0	0	0	0	1	100.00	0.5% Down
0	0	1	0	1	100.00	0.5% Down
1	0	0	0	1	100.00	NO Spread
1	0	1	0	1	100.00	NO Spread

CPU PLL Spread Frequency Selection Table

FSLC B0b2	FSLB B0b1	FSLA B0b0	CPU MHZ	Spread% B0b5=1
0	0	1	133.33	0.5% Down
1	0	1	100.00	0.5% Down

## Amplifier Strap Function

Internal PU w/z 40K ohm

Gain 1	Gain 0	Boost Gain
0	0	6 dB
0	1	12 dB
1	0	18 dB
1	1	24 dB

Schematics Version History Table :

Circuit Ver.	Page	Description	Date
V1.0	9 & 26 & 27	1. change TS Header placement & for S3 Wakeup 2. reserved USB_P13 & USB_N13 Function to TV turner 3. ADD MXM Thermal shutdown 4. ADD Control Bluetooth Switch button	2010-0428

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